VERIFY AND EXTEND VLSI DEVICE MODELS

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The charge-sharing MOS predictor model has been developed and will generate the I-V characteristic of short-channel MOSFETs that are dominated by geometry and field-related effects.

A SPICE2 MOSFET has been developed that represents currents above and below the threshold. The model has been implemented in SPICE2 and extensively tested.

A parameter extraction program has been developed that generates the SPICE2 MOSFET model parameters from either the charge-sharing model or experimental data. This allows investigation of circuit response to process sensitivities without the need to build devices.

The cause of charge nonconservation in SPICE2 has been identified. A new charge model has been developed and implemented in SPICE2 that conserves charge, increases accuracy, and reduces simulation time.

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20. ABSTRACT (continued)

A five-terminal SOI model has been developed. Closed-form expressions for drain current in various regimes of operation as a function of gate, source, drain, substrate, and bulk voltages have been obtained.

The device performance of scaled n-channel and p-channel MOSFETs is theoretically examined down to 0.2-μm gate length. Based on these calculations, some modifications to straightforward scaling are considered.

Other areas of investigation are buried channel MOSFETs with double charge-sharing factors and nonequilibrium effects with history dependence. Low-temperature measurements (to 18°K) reveal no ballistic transport in 0.35-μm gate lengths. A new method of MOSFET capacitance measurement shows nonreciprocal components will have negligible effect on circuit simulations.

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EXECUTIVE SUMMARY

The objectives of the contract were to develop circuit simulation models for SPICE for 1-μm geometry and study the physics of MOS devices to find extensions needed to develop circuit simulation models for submicrometer and SOI devices. The tasks in the initial program were:

Task 1—Fabricate and extensively characterize short-channel (1- to 5-μm) MOSFETs to develop a model,

Task 2—Install and verify the Stanford University process device programs,

These two tasks were completed and an 18-month follow-on was awarded with the following tasks:

Task 3—Model Verification, and

A—Implement charge-sharing model in SPICE for $L \geq 1$ μm

B—Design test chip with benchmark circuits such as flip-flops, clock drivers, etc., to test the model

C—Fabricate and characterize test chip/circuits

D—Extend charge-sharing model to include buried channel devices $L \geq 1$ μm and verify, using test chip devices and circuits

E—Formulate and implement capacitance model based on measured data for short-channel devices.

Task 4—Extension of MOSFET Model to Submicrometer and SOI Devices.

A—Determine inaccuracies of the charge-sharing model for submicrometer ($L \geq 0.3$ μm) and SOI ($L \geq 1$ μm) devices

B—Formulate analytical expressions to improve the accuracy of the charge-sharing model for submicrometer and SOI MOSFETs

C—Investigate the consequences of high field transport on secondary effects in MOSFETs

D—Compare p-channel and n-channel MOSFETs for $L \leq 1$ μm

E—Determine the threshold for onset of ballistic transport effects.

A brief description of the work performed on each task follows.

Task 1

The I-V characteristics of short-channel devices are dominated by geometry and electric field-related effects. These effects have been traditionally modeled using expensive numerical techniques or semiempirical analytical expressions. The charge-sharing MOS predictor developed under this contract models the above physical effects and allows realistic device design iterations at low cost so that process sensitivities of a particular device design may be determined (Chapter II).

Task 2

The Stanford University two-dimensional Poisson solver GEMINI I has been thoroughly investigated. The flexible input capabilities for specifying the device structure and graphics output of the program are important features. Several problems have been identified and are discussed (Chapter XII).

Task 3

Circuit simulations require computationally efficient models. Such a model has been developed that accurately represents the experimental data to within 3 percent over 9 orders of magnitude for currents below and above threshold. The model has been implemented in SPICE2 and extensively tested with no convergence problems or speed penalty compared with the modified Shichman-Hodges model.

An optimal parameter extraction program has also been developed. This establishes a link between the charge-sharing model and the circuit simulation model, allowing the determination of circuit response to process changes without having to build the devices. The parameter extraction program also generates the parameters for a "best fit" of the circuit simulation model to experimental data (Chapters IX, XI).

A buried channel MOSFET model is discussed and a double charge-sharing factor for short-channel devices is derived. Nonequilibrium effects, which have a history dependence, are also discussed (Chapter IV).

A new method for measuring MOSFET capacitances has been developed. Measurements show that the nonreciprocal components of capacitance are small enough to have negligible effect on circuit simulations (Chapter VIII).

The capacitance model presently used in the circuit simulation program SPICE2 does not guarantee conservation of charge and, thus, circuit simulation results can be inaccurate. It has been found that nonconservation of charge in SPICE2 is independent of the device physics of the model and is a result of the way charge is numerically evaluated using capacitance equations. A new charge model has been developed, implemented in SPICE2, and extensively tested. The new model conserves charge, has increased accuracy, and reduces circuit simulation time (Chapter X).

A copy of SPICE with the models developed under this contract, has been delivered to the University of California, Berkeley, which is in the process of implementing and distributing selected portions.

Task 4

A five-terminal silicon-on-insulator MOSFET model has been developed for devices where conduction occurs solely through an inverted channel at the front interface. Closed-form expressions for drain current in various regimes of device operation as a function of gate, source, drain, substrate, and bulk voltage have been obtained. The model has revealed that a heavy doping density generally located at the back interface, though effective in curbing the back interface leakage current, may have a deleterious effect on the driving capability of the device (Chapter III).

Drain-induced primary and secondary impact ionization in short-channel MOSFETs must be anticipated in circuit designs having the debiasing effects of increased substrate current and discharge of nodes in dynamic circuits. These effects have been studied (Chapter VII).

The device performance of scaled n-channel and p-channel MOS devices is theoretically examined in detail down to 0.2-μm gate length, including all of the major effects such as source/drain series resistance, mobility degradation from both parallel and perpendicular fields, and inversion layer capacitance under three different power supply scenarios. From the degradation factor of triode gain and drain saturation current, the relative contribution of each parasitic effect on device performance degradation has been examined. Based on these calculations, some modifications to straightforward scaling are considered (Chapter V).

Low temperature measurements to 18°K with a gate length of 0.35 μm have not produced any evidence of ballistic transport. An interesting phenomenon associated with potential barriers at the source-channel and drain-channel junctions was observed. At low temperatures, a sudden increase of drain current is observed as V_{DS} is increased, which is a result of dependence of avalanche on temperature (Chapter VI).

The programs are written in standard Fortran except graphics, which are based on the HP1000 RTE IV.B operating system. The parameter extraction program and the charge-sharing predictor model are available on request.

SECTION I
INTRODUCTION

Successful completion of an integrated circuit depends on the interaction between the process engineers and the circuit designers. The ideal method of communication between these two groups of people, who often use different vocabularies, would be a computer program that accepts processing parameters as inputs and is capable of generating circuit waveforms from the circuit simulation program SPICE2.

There are conflicting program requirements for these two groups of people. Process engineers are interested in maximizing physical insight into how process changes will alter device characteristics. This requires each physical mechanism to be modeled, resulting in a lengthy computer program in which many complicated mathematical functions must be evaluated. This is acceptable to the process engineer because he will evaluate the I-V characteristics only once for a given process. A circuit designer, however, will utilize the computer model many thousands of times. Thus, cost and model simplicity are of prime importance; physical insight generated by the model is not important as long as the model accurately simulates the device.

The charge-sharing model is discussed in Section II. It meets the needs of the process engineer and could be implemented in SPICE; however, the computer costs for the designer to use this model would be prohibitive. A compromise is to develop a mathematically simple empirical model that is inexpensive for the designer to use. This has been done and is discussed in Section IX. A computer program can then be used to determine the empirical parameters for the designer's model that give a best fit to the charge-sharing model used by the process engineer, thus keeping open the communication link between the process and design engineers. Such a translation program for finding the empirical model constants has been developed and is discussed in Section XI. The user's manuals for these programs and for a plotting program to display output of the models are discussed in Appendixes I and J. The programs are currently running on an HP1000 and are written in Fortran.

Sections II through VIII discuss other technological aspects of MOSFETs that have been modeled but are not currently in the charge-sharing program. These include silicon-on-insulator (SOI) and buried channel devices. A comparison of p- and n-channel devices is of interest as scaling reduces the advantages of the n-channel MOSFET over the p-channel device. Low-temperature measurements did not reveal any effects of ballistic transport but did uncover an interesting effect of potential barriers at the edge of the gate. A unique method for measuring MOS capacitances indicates that the nonreciprocal components exist but are not significant for circuit simulation.

Other aspects of numerical modeling are discussed in Sections X and XII. The problem of charge nonconservation in the circuit simulation program SPICE2 has been identified, solved, and verified by implementation in SPICE2. The Stanford University program GEMINI was also analyzed in detail and is discussed in Section XII.

SECTION II

CHARGE-SHARING MOS PREDICTOR MODEL

Submicrometer ($L > 0.5\ \mu m$) MOSFETs show considerable geometry dependence in their I-V characteristics. First-principles models of submicrometer devices[1,2] have been based on numerical simulations that are expensive and not suitable for circuit and process design iterations. An analytic model for short-channel MOSFETs has been developed that predicts I-V characteristics of FETs with $L > 0.5\ \mu m$ from process and structure data. The current voltage predictions are verified as accurate within the statistical tolerance of these process and structure parameters, thus providing a powerful tool to use for process design and parameter sensitivity studies with desktop computers at extremely low cost and very high throughput.

Such an analytical model, which may be run on desktop calculators such as the HP 9545, will find an excellent application in the design of short-channel MOSFETs for specific circuit applications. As Figure 1 shows, this program permits realistic device design iterations at very low cost so that process sensitivities of a particular device design may be determined. It is possible to establish the gate oxide thickness doping profiles and operating voltage tradeoffs without involving expensive process iterations, thus permitting a sharp reduction in the development cost of a scaled MOSFET technology. Device designs will be modeled exclusively to achieve optimum circuit performance for a given application, since the output from the charge-sharing model can be translated into a computationally efficient SPICE2 model discussed in Section IX by using the model-fitting program discussed in Sections XI and XIV.

The starting point for the model is the familiar long-channel equation

$$I_D = \mu Co \frac{W}{L}\left\{\left(V_{GS} - V_{fb} - 2\phi_f - \frac{V_{DS}}{2}\right)V_{DS}\right\} \\ \frac{-2F}{3Co}\sqrt{2\epsilon q N_A}\ \left[(V_{DS} + V_{BS} + 2\phi_F)^{3/2} - (V_{BS} + 2\phi_F)^{3/2}\right] \tag{1}$$

where the charge-sharing factor, F, has been added. The following sections describe how the mobility, charge-sharing factor, and doping concentration are modeled for short-channel devices.

The current at the saturation voltage is evaluated by setting V_{DS} in Equation (1) equal to V_{DSAT}. The current in the saturation region is then given by

$$I_D = \frac{I_{DSAT}}{\left(1 - \frac{\Delta L}{L}\right)} \tag{2}$$

The total current is then evaluated by adding the above threshold component and the subthreshold component.

A. Charge-Sharing Factor

A method to convert the two-dimensional short-channel problem into a one-dimensional problem was first proposed by Poon, et al.,[3] and later extended by Taylor.[4,5] Initially, our approach was to use

[1]M.S. Mock, "A Two-Dimensional Mathematical Model of the Insulated-Gate Field-Effect Transistor," *Solid State Electronics*, **16** (1973), p. 601.

[2]P.E. Cottrell and E.M. Buturla, *Numerical Analysis of Semiconductor Devices*, ed. by B.T. Browne and J.H. Miller (Bode Press, Dublin, 1979).

[3]H.C. Poon, L.D. Yau, R.L. Johnston, and D. Beecham, "DC Model for Short-Channel IGFETS," paper 8.4 presented at IEEE Int. Electron Devices Meet., Washington, D.C. (1973).

[4]G.W. Taylor, "The Effects of Two-Dimensional Charge-Sharing on the Above-Threshold Characteristics of Short-Channel IGFETS," *Solid State Electronics*, **22** (1979), p. 701.

[5]G.W. Taylor, "Subthreshold Conduction in MOSFETs," *IEEE Trans. Electron Devices*, **ED-25** (1978), p. 337.

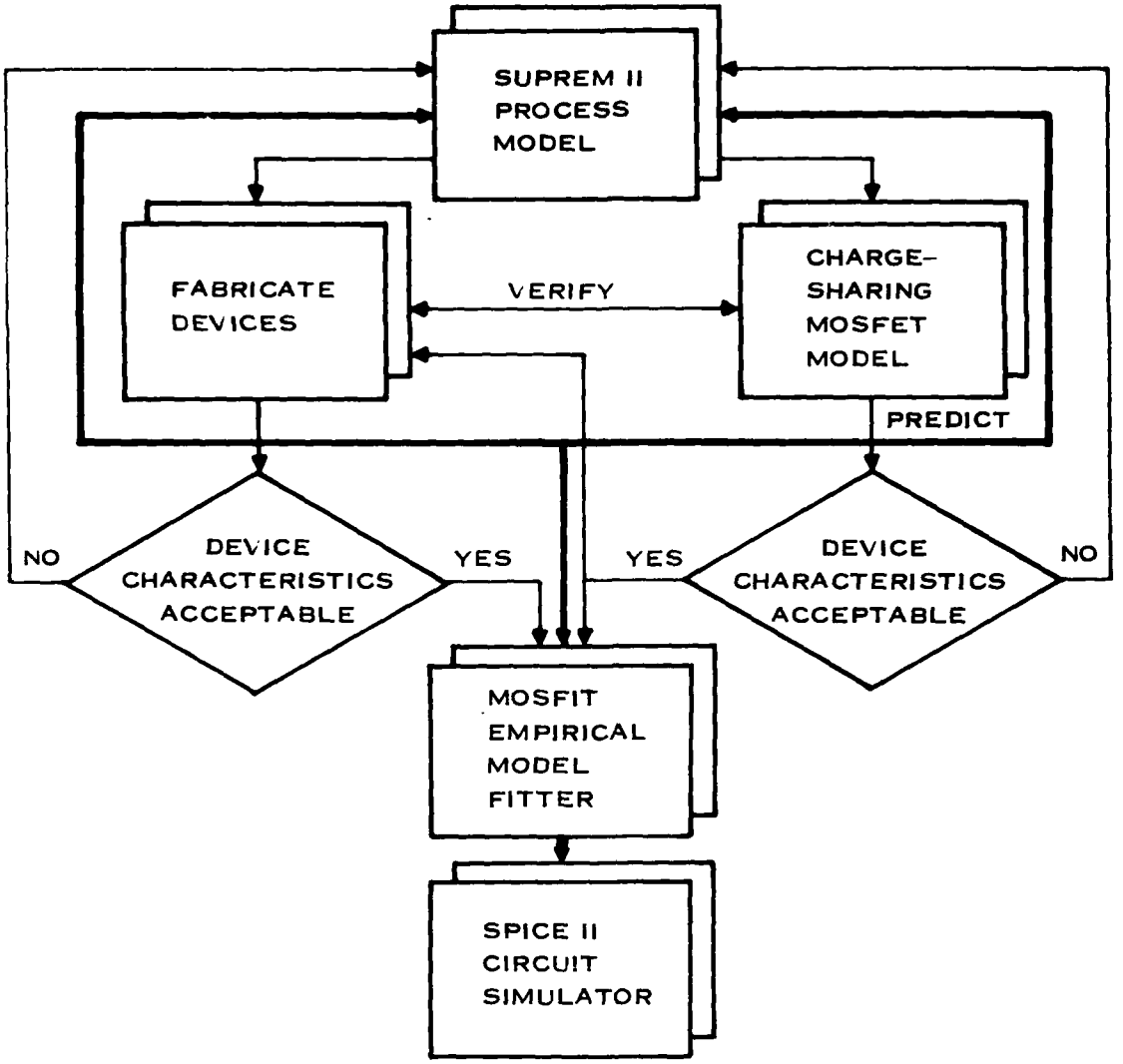


Figure 1. Flow Diagram for the Use of a Predictor Model for Device Design

Taylor's results; however, it was found that for a small range of drain bias near $V_{DS} = 0$, the threshold voltage would increase with increasing V_{DS} owing to the wrong functional dependence of the charge-sharing factor.

The approach of Sun and Moll[6] more closely approximates the physical situation by using a quadrangle to define the depletion charge associated with the gate rather than a trapezoid, which is used in the previously mentioned models. The derivation here follows a similar approach.

[6]E. Sun and J. Moll, "A Simple Analytical Short Devices, Channel MOS Model," *IEEE Trans. Electron Devices*, **ED-26** (1978), p. 461.

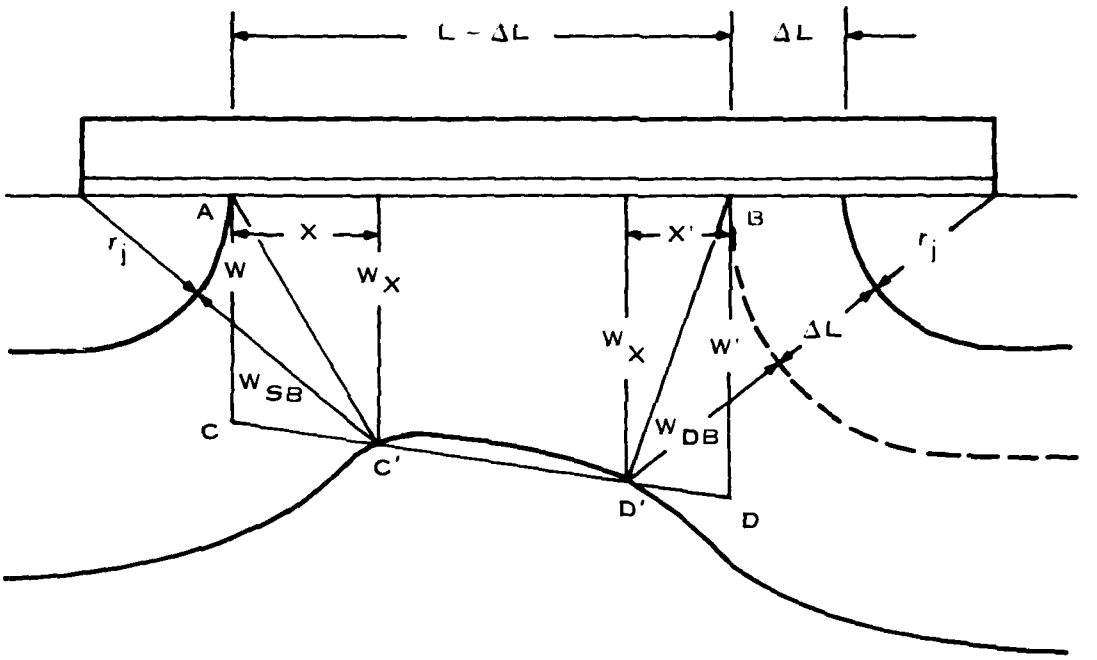


Figure 2. Charge-Sharing Factor for a Saturation Region

Referring to Figure 2, the charge-sharing factor for a MOSFET in saturation can be defined as

$$F = \frac{\text{area } (ABC'D')}{\text{area } (ABCD)} = \frac{\dfrac{(W + W')(L - \Delta L)}{2} - \dfrac{WX}{2} - \dfrac{W'X'}{2}}{\dfrac{(W + W')(L - \Delta L + 2\delta)}{2}} \tag{3}$$

where $\delta = t_{ox}/2\pi \ln (\pi \text{ e } L/t_{ox})$ is the fringing length.[3]

W and W' are depletion layer widths associated with the surface potential at the source and pinchoff points of the channel ignoring the effects of the source and drain diffusions.

$$W = \sqrt{K (V_{BS} + 2\phi_F)} \tag{4}$$

$$W' = \sqrt{K (V_{DSAT} + V_{BS} + 2\phi_F)} \tag{5}$$

W_x and X are computed as follows:

$$W_x = W + X\left(\frac{W' - W}{L - \Delta L}\right) \tag{6}$$

and

$$(r_j + X)^2 + W_x^2 = (r_j + W_{SB})^2 \tag{7}$$

where W_{SB} is the source diffusion depletion region and is computed using the planar junction approximation

$$W_{SB} = \sqrt{K\,(V_{BS} + V_{bi})} = W \tag{8}$$

where it has been assumed that $V_{bi} = 2\,\phi_F$. Solving (6) and (7) simultaneously and using (8) yields

$$X = -\frac{\left[r_j + W\left(\frac{W' - W}{L - \Delta L}\right)\right] + \sqrt{\left[r_j + W\left(\frac{W' - W}{L - \Delta L}\right)^2\right] + 2\,r_j\,W\left[1 + \left(\frac{W' - W}{L - \Delta L}\right)^2\right]}}{\left[1 + \left(\frac{W' - W}{L - \Delta L}\right)^2\right]} \tag{9}$$

Following the same approach it can be shown that

$$W'_x = W' - X'\left(\frac{W' - W}{L - \Delta L}\right) \tag{10}$$

and

$$X' = -\frac{\left[r_j + \Delta L - W'\left(\frac{W' - W}{L - \Delta L}\right)\right] + \sqrt{\left[r_j + \Delta L + W'\left(\frac{W' - W}{L - \Delta L}\right)\right]^2 + 2W'(r_j + \Delta L)\left[1 + \left(\frac{W' - W}{L - \Delta L}\right)^2\right]}}{\left[1 + \left(\frac{W' - W}{L - \Delta L}\right)^2\right]} \tag{11}$$

Equations (3), (6), and (10) can be solved to give

$$F = \frac{\left[L - \Delta L - \frac{WX + X^2\left(\frac{W' - W}{L - \Delta L}\right)}{(W + W')}\right] - \frac{W'X' - X'^2\left(\frac{W' - W}{L - \Delta L}\right)}{(W + W')}}{(L - \Delta L + 2\delta)} \tag{12}$$

Equations (4), (5), (9), (11), and (12) are used to complete F in the saturation region. The calculation of F in the linear region is accomplished by replacing V_{DSAT} with V_{DS} and setting $\Delta L = 0$.

B. EXTENSION OF THE CHARGE-SHARING FACTOR TO NEAR PUNCH-THROUGH

If the bias conditions are such that the points C' and D' are coincident in Figure 2, the quadrangle then reduces to a triangle. Any change in the bias conditions that causes further overlap of the source and drain depletion layers will result in a reduction of the area of the triangle as shown in Figure 3. The charge-sharing factor for Figure 3 is

$$F = \frac{\text{area } (ABE)}{\text{area } (ABCD)} = d\,\frac{(L - \Delta L)/2}{(W + W')\,(L - \Delta L + 2\delta)/2} \tag{13}$$

From the geometry of Figure 1 it can be shown that

$$d = \frac{L - \Delta L}{(X/W_x + X'/W'_x)} \tag{14}$$

resulting in

$$F = \frac{(L - \Delta L)^2\,W_x W'_x}{(W + W')\,(XW'_x + X'W_x)\,(L - \Delta L + 2\delta)} \tag{15}$$

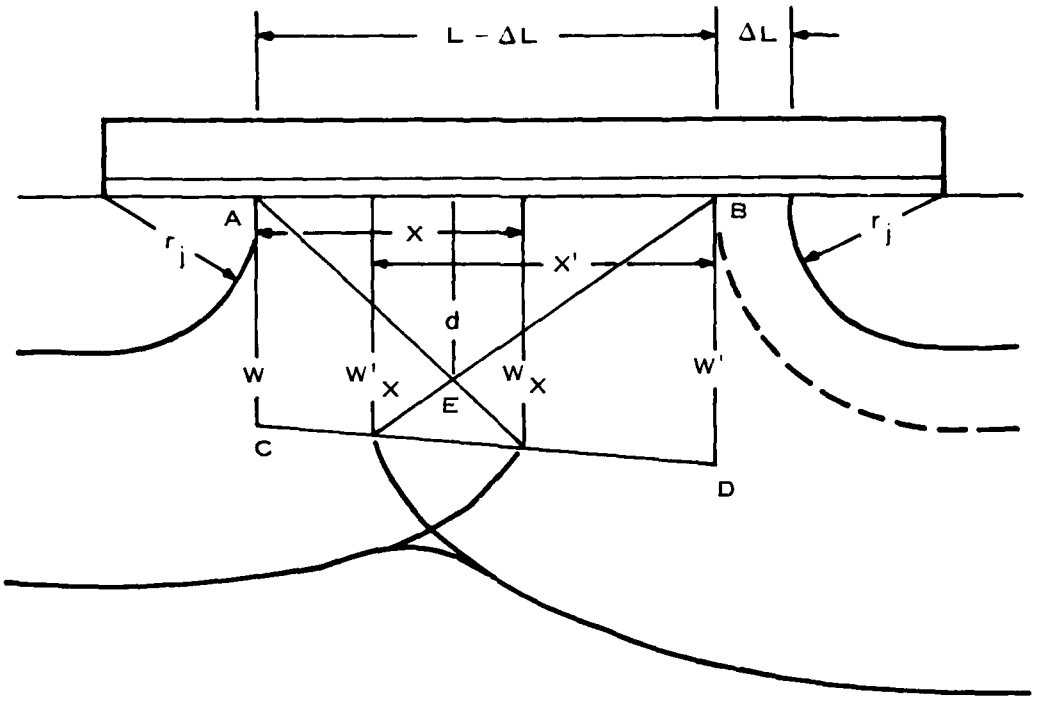


Figure 3. Charge-Sharing Factor Near Punch-Through Operation

for the saturation region. The linear region F near punch-through is obtained by setting $\Delta L = 0$.

C. DYNAMIC AVERAGE DOPING TRANSFORMATION

Designs of n-MOS circuits, particularly for dynamic and analog applications, require the accurate modeling of the body effect, especially for precharging devices. While accurate models for long-channel devices with ion-implanted channel doping have been reported,[7] the two-dimensional CAD short-channel MOSFET models[4,8] generally use an average constant doping in the channel region. This simplification is required because it results in an analytical formulation of the problem suitable for CAD simulators such as SPICE. Such models are quite accurate if the depth of the ion-implanted region is small compared to the total depletion depth in the substrate bias range of interest, or if the depletion depth is always confined to a small fraction of the implanted layer. The trend toward higher voltage bootstrap modes and requirements of lower diffusion line capacitance,[9] however, have necessitated the design of channel ion implants that result in a depletion region depth comparable to the implant depth in the source-to-substrate bias range of interest (Figure 4). In these cases, the constant average doping approximation results in a serious error in the calculation of substrate sensitivities since $N_{A\,eff}$ may be determined by the implant for low V_{BS} (substrate bias) and by the background level for larger V_{BS}.

We propose a dynamic average doping approximation, which is a function of substrate bias, so the averaging over the nonuniform ion-implanted doping and the substrate region may be simply represented.

[7]R.R. Troutman, "Ion Implanted Threshold Tailoring for IGFETs," *IEEE Trans. Electron Devices*, **ED-24** (1977), p. 182.

[8]L.D. Yau, "A Simple Theory to Predict the Threshold Voltage of Short Cchannel IGFETs," *Solid-State Electronics*, **17** (1974), p. 1059.

[9]E.A. Reese, L.S. White, N. Hong, D.J. Redwine, J.C. McAlexander, and G.R. Mohan Rao, "Sub100ns 16k×1 MOS dRAM Using a Grounded Substrate," *IEEE International Electron Devices Digest of Technical Papers* (1979), p. 355.

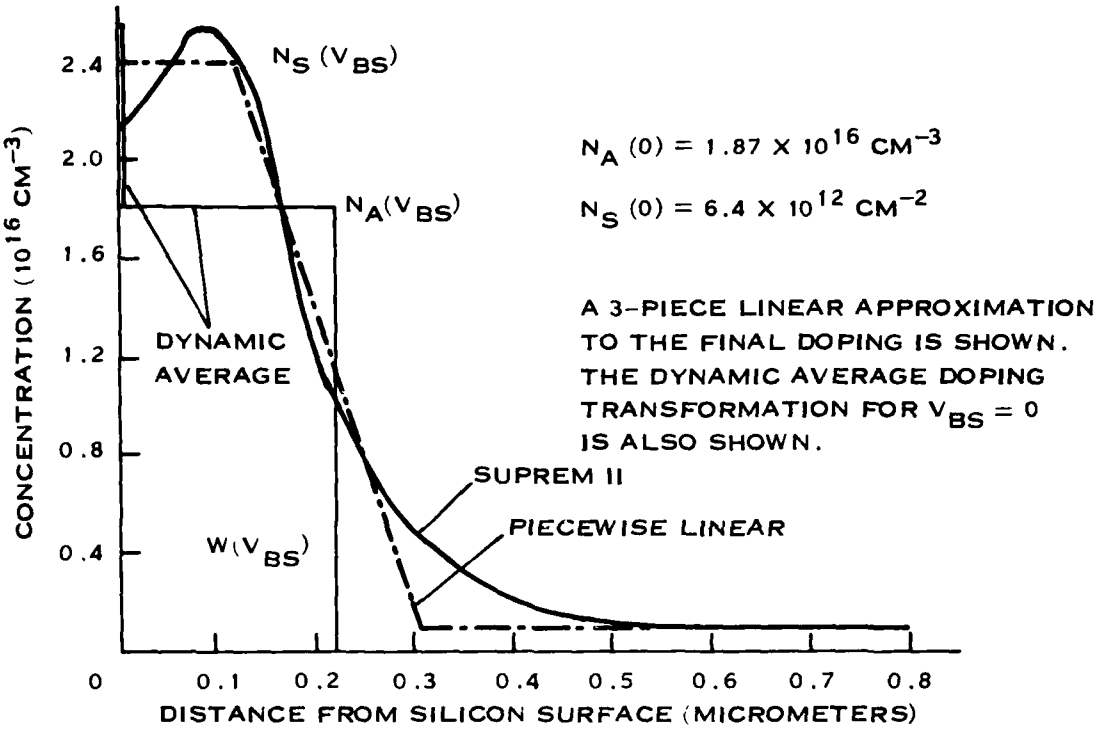


Figure 4. Typical Channel Doping Profile for an Ion Implanted MOSFET After All Process-Related Heat Treatment is Calculated From SUPREM II Process Simulation

Dynamic averaging of the doping with substrate bias may, in principle, be applied to any arbitrary doping profile within the bounds of the depletion approximation. Depletion layer width $W(V_{BS})$ at given source-to-substrate bias V_{BS} may be calculated for $\phi_s \approx 2\phi_f(0)$, the Fermi level corresponding to the doping at the surface. We may now define the equivalent dynamic average doping $N_A(V_{BS})$, which results in an equal depletion layer width, so that all geometry-related effects may be calculated.

$$N_A(V_{BS}) = \left(\frac{2\epsilon_S}{q}\right) \frac{[V_{BS} + 2\phi_f(0)]}{[W(V_{BS})]^2} \tag{16}$$

Equation (16) guarantees the depletion depth in the equivalent model will represent the true depletion depth in the implanted device. However, the total charge in the depletion layer must also be conserved. We conserve the total charge by defining a surface charge $N_S(V_{BS})$ so that

$$N_S(V_{BS}) = \int_0^W N(x)dx - N_A(V_{BS})\, W(V_{BS}) \tag{17}$$

Thus, the transformation proposes the redistribution of the total depletion charge into a surface component and a uniform doping that maintains the depletion depth. It is interesting to examine the limiting cases of this transformation. At low substrate bias (Figure 4) the depletion width is near the surface, and the average doping is determined by the distribution of the implanted charge. As the substrate bias is increased, the depletion layer edge moves beyond the implanted region. The average doping level approaches the substrate doping, and the implanted charge is associated as a surface layer charge only. The transformed impurity distribution may be used to compute short-channel characteristics using the charge-sharing model. The threshold voltage of the MOSFET in the charge-sharing formulation is written as

$$V_T = V_{fb}(0) + \frac{F[N_A(V_{BS})]}{C_o}\left\{qN_S(V_{BS}) + \sqrt{2\epsilon_S qN_A(V_{BS})\,[V_{BS} + 2\phi_f(0)]}\right\} \tag{18}$$

where $F[N_A(V_{BS})]$ is the charge-sharing factor, which accounts for the geometry dependence. The calculation of two-dimensional effects in short-channel MOSFETS using this dynamic doping average transformation, assumes that the depth distribution of the channel-depletion charge may be ignored. This appears, at first, to be a crude approximation; however, it is the integrated total bulk charge that affects the current in a MOSFET. Therefore, this approximation, which conserves charge and geometry, should apply.

As an example of the validity of the dynamic average substrate doping transformation in the charge-sharing short-channel model, we examine the substrate sensitivity of MOSFETs with three different channel lengths. The experimental measurement of threshold voltage is performed in the linear region with V_{DS} = 50 mV. The doping profile shown in Figure 4 is the channel doping of the measured devices as calculated from SUPREM II, including the effects of heat treatment. For this typical class of profiles, a three-piece linear doping distribution fits satisfactorily. Thus, for single-peak final doping profiles after processing, the problem may be simplified even further. The solution of Poisson's equation for the piecewise linear doping may be obtained analytically, thereby making the dynamic average doping transformation even more attractive for CAD modeling. The results of the threshold calculation for MOSFETs with channel lengths of 16.0, 2.5, and 1.1 μm are compared with experimental data in Figure 5. The good agreement for the long-channel device represents the validity of the average doping transformation for calculation of threshold voltages in an ion-implanted device. The predictions of the substrate sensitivity on short-channel devices also agree with measured data. This demonstrates that the charge-sharing

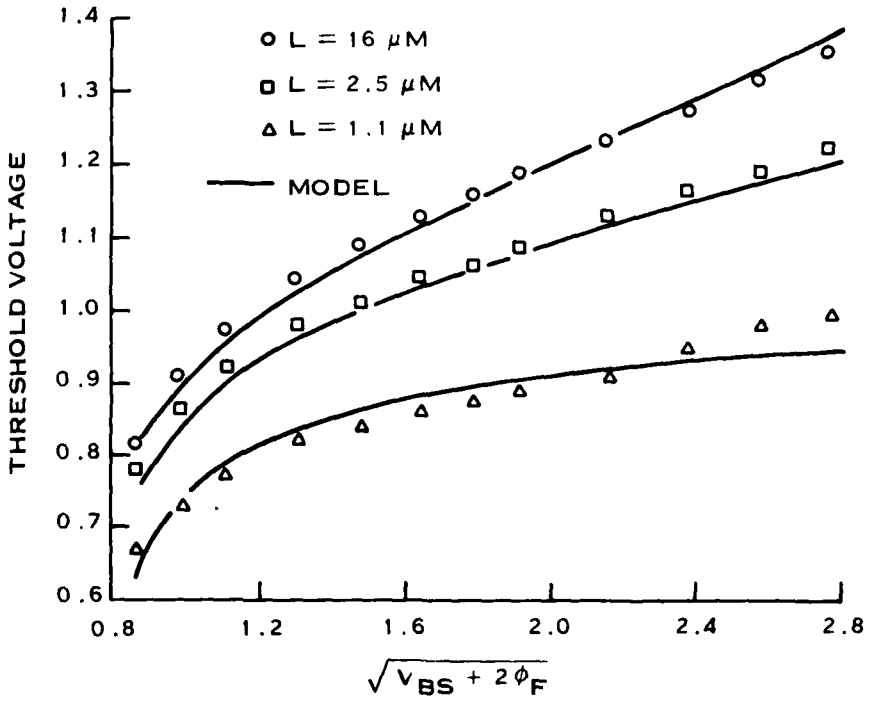


Figure 5. Substrate Sensitivity of MOSFETs Fabricated With Channel D Opens as Measured on Devices of Various Channel Length, Compared With the Dynamic Average Doping Theory

formulation for short-channel MOSFETs may be used with the dynamic average substrate doping concentration to obtain analytic solution to the short-channel problem in MOSFETs with nonuniform channel doping.

As a first attempt at extending the dynamic average doping transformation (DADT) to the calculation of the device current, the value of $N_A(V_{BS}, V_{DS} = 0)$ was used to calculate the charge-sharing factor $F(V_{BS}, V_{DS}, N_A)$. Also, the surface charge was defined as

$$N_S(V_{BS}) = \int_0^W N(x)dx - N_A(V_{BS}, V_{DS} = 0)\ W(V_{BS}, V_{DS} = 0) \tag{19}$$

The surface charge was then treated as if it were additional Q_{SS}, and thus a new flatband voltage was defined as

$$V_{fb} = V_{fb0} + \frac{F(V_{BS}, V_{DS}, N_A)\ qN_S(V_{BS})}{C_o} \tag{20}$$

The current could then be written as

$$I_D = \mu C_o \frac{W}{L}\left\{\left(V_{GS} - V_{fb} - 2\phi_f - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2F(V_{BS}, V_{DS}, N_A)\sqrt{2\epsilon\, qN_A}}{3C_o}\right. \tag{21}$$

$$\left. \cdot\ [(V_{DS} + V_{BS} + 2\phi_f)^{3/2} - (V_{BS} + 2\phi_f)^{3/2}]\right\}$$

This formulation results in computationally simple closed form expressions, which was the reason for attempting this approach.

On closer examination, it was found for long-channel devices with a fixed, but large, V_{DS} that the drain current initially increased as the magnitude of V_{BS} increased and then began to decrease with continued increase in the magnitude of V_{BS}. This is clearly a nonphysical situation, which is caused by computing $N_A(V_{BS})$ and $N_S(V_{BS})$ under the condition that $\phi_S = 2\phi_f$, which is equivalent to calculating them at the source. $N_S(V_{BS})$ is defined as part of V_{fb}. This implicitly assumes that $N_S(V_{BS})$ is constant across the channel length and is thus independent of V_{DS}. The calculation of the bulk charge using $N_A(V_{BS})$ does not neglect V_{DS}, because the depletion layer edge may vary along the channel even though $N_A(V_{BS})$ is assumed independent of V_{DS}. These different functional dependences of $N_S(V_{BS})$ and $N_A(V_{BS})$ on V_{DS} result in nonconservation of charge in this approach, which is most easily observed by the dependence of I_D on V_{BS}. For short-channel devices the variation of the charge-sharing factor F with the terminal voltages may mask this nonphysical response.

The concept of the DADT is useful for the prediction of threshold voltage because $V_{DS} = 0$ and a value of N_A is obtained that permits an accurate calculation of the charge-sharing factor F. However, the DADT is not simply extended to the case where $V_{DS} \neq 0$. What is required is to solve the integral over V_{DS} in Equation (22).

$$I_D = \mu C_o \frac{W}{L}\left\{\left(V_{GS} - V_{fbo} - 2\phi_f - \frac{V_{DS}}{2}\right)V_{DS} - \frac{F}{C_o}\int_0^{V_{DS}} Q(V_y)\, dV_y\right\} \tag{22}$$

This has been done for a four-piece linear fit to the channel profile as illustrated in Figure 6. Solution of Poisson's equation results in the following expressions for the depletion layer depth, W.

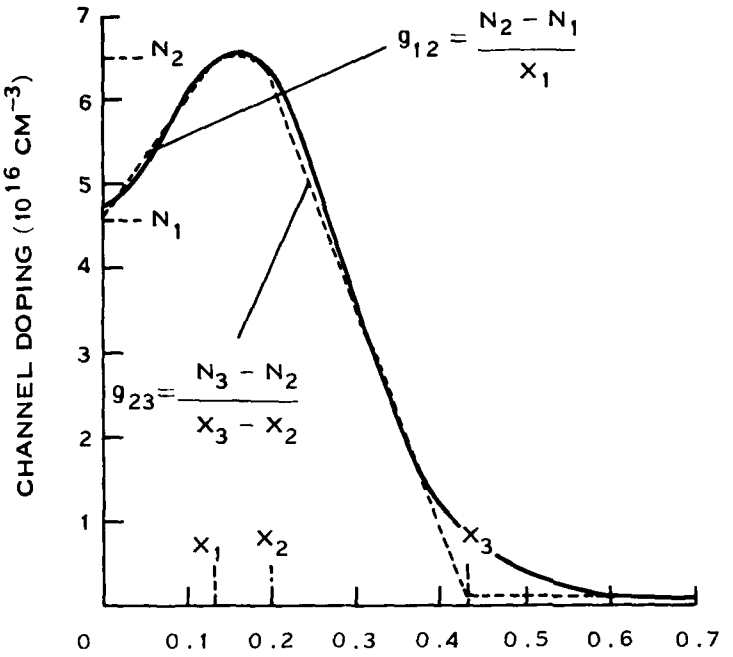


Figure 6. Four Piece Linear Fit to Channel Doping Profile Calculated From SUPREM II

For $0 \leq W \leq X_1$

$$\left[\frac{qg_{12}}{3\epsilon_S}\right] W^3 + \left[\frac{qN_1}{2\epsilon_S}\right] W^2 - (V_y + V_{BS} + 2\phi_F) = 0 \tag{23}$$

For $X_1 \leq W \leq X_2$

$$\left[\frac{qN_2}{2\epsilon_S}\right] W^2 + \left[\frac{-g_{12}X_1^3}{6\epsilon_S} - (V_y + V_{BS} + 2\phi_F)\right] = 0 \tag{24}$$

For $X_2 \leq W \leq X_3$

$$\left[\frac{qg_{23}}{3\epsilon_S}\right] W^3 + \left[\frac{qN_2}{2\epsilon_S} - \frac{qg_{23}X_2}{2\epsilon_S}\right] W^2 + \left[\frac{-qg_{12}X_1^3}{6\epsilon_S} + \frac{qg_{23}}{6\epsilon_S} X_2^3 - (V_y + V_{BS} + 2\phi_F)\right] = 0 \tag{25}$$

For $W \geq X_3$

$$\left[\frac{qN_3}{2\epsilon_S}\right] W^2 + \left[\frac{-qg_{12}X_1^3}{6\epsilon_S} + \frac{qg_{23}X_2^3}{6\epsilon_S} - \frac{qg_{23}X_2X_3^2}{2\epsilon_S} + \frac{qN_2X_3^2}{2\epsilon_S} + \frac{qg_{23}X_3^3}{3\epsilon_S} - \frac{qN_3X_3^2}{2\epsilon_S} - (V_y + V_{BS} + 2\phi_F)\right] = 0 \tag{26}$$

Explicit expressions for W in Equations (24) and (26) are straightforward. For Equations (23) and (25), the expressions are somewhat more complex. If we assume the cubic equations have the form

$$aW^3 + bW^2 + d = 0$$

then for $0 \leq W \leq X_1$, $-27da^2 \leq 4b^3$ and $g_{12} > 0$

$$W = \frac{2}{3}\left|\frac{b}{a}\right| \cos\left\{\frac{1}{3}\arccos\left[\frac{-2\left(\frac{b}{a}\right)^3 + 27\left(\frac{d}{a}\right)}{2\left|\frac{b}{a}\right|^3}\right]\right\} - \frac{b}{3a} \tag{27}$$

and for $0 \leq W \leq X_1$ with $-27da^2 \geq 4b^3$ and $g_{12} > 0$

$$W = \frac{2}{3}\left|\frac{b}{a}\right| \cosh\left\{\frac{1}{3}\operatorname{arccosh}\left[\frac{-\left[2\left(\frac{b}{a}\right)^3 + 27\left(\frac{d}{a}\right)\right]}{2\left|\frac{b}{a}\right|^3}\right]\right\} - \frac{b}{3a} \tag{28}$$

When $X_2 < W < X_3$ and $g_{12} < 0$, find

$$W = -\frac{2}{3}\left|\frac{b}{a}\right| \cos\left\{\frac{1}{3}\arccos\left[\frac{-\left[2\left(\frac{b}{a}\right)^3 + 27\left(\frac{d}{a}\right)\right]}{2\left|\frac{b}{a}\right|^3}\right] + \frac{\pi}{3}\right\} - \frac{b}{3a} \tag{29}$$

Note that the region $0 \leq W \leq X_1$ has two possible solutions. Both of these solutions may be required when integrating over V_{DS}. To illustrate the solution method, let us examine the region $X_2 \leq W \leq X_3$.

$$Q_{B13} = \int_{V_2}^{V_3} Q(V_y) = q \int_{V_1}^{V} \left[N_1 W(V_y) + \frac{1}{2} g_{12} W^2(V_y)\right] dV_y \tag{30}$$

Equation (29) can be put in the form

$$W(V_y) = A \cos\left\{\frac{1}{3}\arccos(I + JV_y) + \frac{\pi}{3}\right\} - B \tag{31}$$

So we need to solve integrals of the form

$$\int \cos\left\{\frac{1}{3}\arccos(I + JV_y) + \frac{\pi}{3}\right\} dV_y \tag{32}$$

and

$$\int \cos^2\left\{\frac{1}{3}\arccos(I + JV_y) + \frac{\pi}{3}\right\} dV_y \tag{33}$$

These can be solved by making the substitution

$$u = \frac{1}{3}\arccos(I + JV_y) \tag{34}$$

so

$$dV_y = -\frac{3 \sin(3u)\, du}{J} \tag{35}$$

The final solution is too long to reproduce here. It has been incorporated into the charge-sharing program and is easily evaluated. The subroutines doing these computations have all been verified by comparison with numerical solutions.

The problem that remains is to determine the value of N_A to use in the calculation of the charge-sharing factor F. Clearly, the value of N_A calculated at the source is too large, while the value calculated at the drain is too small. At present, the charge-sharing program user can select the fraction, X, of V_{DS} at which the effective doping N_A for the charge-sharing factor, $F[V_{BS}, V_{DS}, N_A(V_{BS}, X \cdot V_{DS})]$, is determined.

D. MOBILITY AND SATURATION VOLTAGE

We define the functional form of the mobility[10] as

$$\mu(V_{DS}, V_{GS}, V_{BS}) = \frac{\mu(V_{GS}, V_{BS})}{\left(1 + \frac{1}{E_C}\frac{d\phi}{dy}\right)} \tag{36}$$

$$\mu(V_{GS}, V_{BS}) = \frac{\mu_o}{1 + \theta\left(V_{GS} - V_T + \frac{2}{C_o}\sqrt{\frac{2\epsilon_S}{qN_A}(V_{BS} + 2\phi_F)}\right)} \tag{37}$$

where μ_o is the low field mobility and θ represents the effects of surface scattering and scales with the oxide thickness. The mobility will decrease with increasing V_{BS} in agreement with the results of Sabnis and Clemens.[11] Thus, the expression for current becomes

$$I_D = \frac{Wq\mu\,(V_{GS}, V_{BS})}{\left(1 + \frac{1}{E_c}\frac{d\phi}{dy}\right)} \cdot \frac{d\phi}{dy} \tag{38}$$

Rearranging gives

$$\frac{I_D}{W} = \left[q\mu\,(V_{GS}, V_{BS})\,n - \frac{I_D}{WE_c}\right]\frac{d\phi}{dy} \tag{39}$$

Substituting

$$qn = C_o\,(V_{GS} - V_{FB} - 2\phi_F - V_y) - \sqrt{2\epsilon_s\,qN_A\,(V_y + V_{BS} + 2\phi_F)} \tag{40}$$

into Equation (39) and then integrating and rearranging gives

$$I_D = \frac{\mu(V_{GS}, V_{BS})\,C_o\,W}{\left(1 + \frac{V_{DS}}{LE_c}\right)L}\left\{\left(V_{GS} - V_{FB} - 2\phi_F - \frac{V_{DS}}{2}\right)V_{DS}\right. \tag{41}$$

$$\left. - \frac{2F}{3\,C_{ox}}\sqrt{2\epsilon_s qN_A}\;\;[(V_{DSAT} + V_{BS} + 2\phi_F)^{3/2} - (V_{BS} + 2\phi_F)^{3/2}]\right\}$$

There are two possible approaches to determining the saturation voltage. The first approach is to examine Equation (38) in the limit of very large electric fields. This gives

$$\text{limit } I_D = Wq\mu(V_{GS}, V_{BS})\,E_c\,n \tag{42}$$

$$\frac{d\phi}{dy} \to \infty$$

where n is determined from the threshold voltage at the drain to be

$$n = \frac{C_o}{q}\left[V_{GS} - V_{FB} - 2\phi_F - \frac{\sqrt{2\epsilon qN_A}}{C_o}\sqrt{V_{DSAT} + V_{BS} + 2\phi_F}\right] \tag{43}$$

Note that Equation (42) does *not* imply that the carriers are moving in an electric field E_C because this expression was obtained by letting the electric field become infinite. The saturation voltage can then be determined by setting Equation (41) with $V_{DS} = V_{DSAT}$ equal to Equation (42), which, after rearranging gives

[10]M.H. White, F. Van De Wiele and J.P. Lambot, "High Accuracy MOS Models for Computer-Aided Design," *IEEE Trans. Electron Devices*, **ED-27** (May 1980), p. 899.

[11]A.G. Sabnis and J.T. Clemens, "Characterization of the Electron Mobility in the Inverted <100> Si Surface," *IEDM Tech. Digest* (December 1979), pp. 18–21.

$$(LE_c + V_{DSAT})\left[V_{GS} - V_{FB} - 2\phi_F - \frac{1}{C_o}\sqrt{2\epsilon qN_A\,(V_{DSAT} + V_{BS} + 2\phi_F)} - V_{DSAT}\right]$$

$$= \left(V_{GS} - V_{FB} - 2\phi_F - \frac{V_{DSAT}}{2}\right)V_{DSAT} - \frac{2_F}{3C_o}\sqrt{2\epsilon qN_A}\left[(V_{DSAT} + V_{BS} + 2\phi_F)^{3/2}\right. \tag{44}$$

$$\left. - (V_{BS} + 2\phi_F)^{3/2}\right]$$

The second approach is to differentiate Equation (41) with respect to V_{DS} and set it equal to 0. This will identically yield Equation (44). Thus, these two approaches are identical, i.e., the charge goes to 0 and the electric field becomes infinite at the drain.

We know physically that the charge cannot go to 0 and the electric field cannot become infinite. Let us then set the electric field in equation (38) to a maximum value, E_{MAX}, corresponding to the saturation voltage, set this expression equal to Equation (41) evaluated at $V_{DS} = V_{DSAT}$ to obtain

$$V_{DSAT} = \frac{-B + \sqrt{B^2 - 4AC}}{2A} \tag{45}$$

where

$$A = \left(\frac{E_{MAX}}{E_c + E_{MAX}}\right) - \frac{1}{2}$$

$$B = (V_{GS} - V_{FB} - 2\phi_F)\frac{LE_c}{(E_c + E_{MAX})} - \frac{E_{MAX}}{(E_c + E_{MAX})}[V_{GS} - V_{FB} - 2\phi_F$$

$$- \frac{1}{C_o}\sqrt{2\epsilon qN_A\,(V_{GST} + V_{BS} + 2\phi_F)}]$$

$$C = -\frac{2_F}{3\,C_{ox}}\sqrt{2\epsilon qN_A}\;\;[(V_{GST} + V_{BS} + 2\phi_F)^{3/2} - (V_{BS} + 2\phi_F)^{3/2}]$$

$$- \left(\frac{LE_c\,E_{MAX}}{E_c + E_{MAX}}\right)\left[V_{GS} - V_{FB} - 2\phi_F - \frac{1}{C_o}\sqrt{2\epsilon qN_A\,(V_{DSAT} + V_{BS} + 2\phi_F)}\right]$$

where $V_{GST} = V_{GS} - V_T$ is the initial estimate for the saturation voltage. Better estimates of the saturation voltage are obtained by substituting the calculated value of V_{DSAT} into V_{GST} and recomputing V_{DSAT}.

E. CHANNEL LENGTH MODULATION

Figure 7 shows the feedback mechanism that is principally recognized as the reason for finite channel conductance in saturation. At drain voltages greater than V_{DSAT} the pinchoff point moves away from the drain by a distance ΔL so that the drain current is increased by

$$I_d = \frac{I_{DSAT}}{(1 - \Delta L/L)} \tag{46}$$

Calculations of the channel length modulation L have been attempted by several authors[12,13,14] and the simplest formulation is based on an electrostatic screening which derives

[12]G. Merckel, J. Borel, and N.F. Cupcea, "An Accurate Large Signal MOS Transistor Model for Use in CAD," *IEEE Trans. Electron Devices*, **ED-19** (1972), p. 681.

[13]D. Frohman-Bentchkowsky and A.S. Grove, "Conductance of MOS Transistors in Saturation," *IEEE Trans. Electron Devices*, **ED-16** (1969), p. 108.

[14]V.G.K. Reddi and C.T. Sah, *IEEE Trans. Electron Devices*, **ED-12** (1965), p. 139.

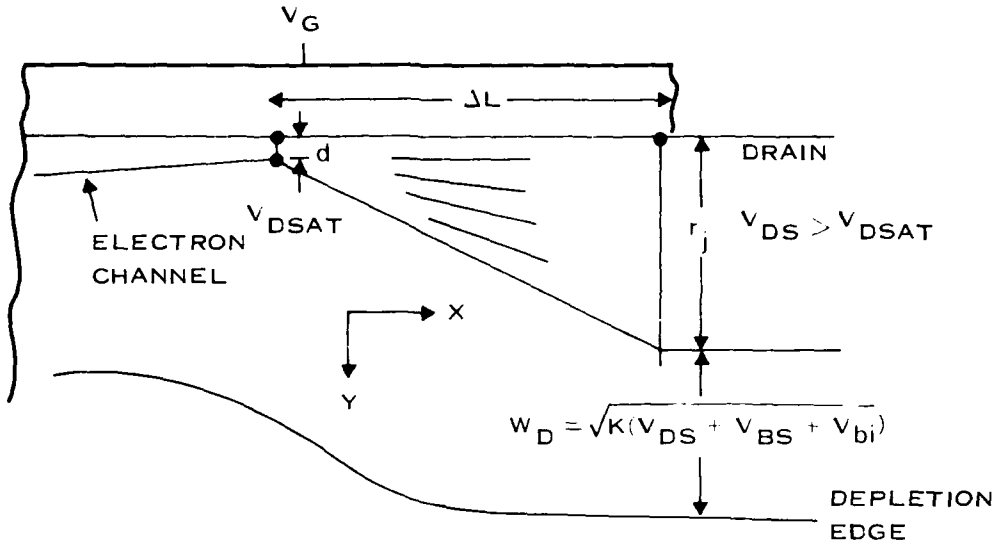


Figure 7. Current-Spreading Model for Channel Length Modulation

$$\Delta L = \sqrt{K (V_{DS} - V_{DSAT})} \tag{47}$$

This expression is quite valid for drain currents at which the electron density near the drain is significantly less than the bulk charge density. As an example, let us estimate the drain current level at which this assumption holds good. For a typical transistor with $L \sim 1.5\ \mu$m, the substrate doping is about 10^{16} cm^{-3}. For $W = 1\ \mu$m, $r_j = 0.4\ \mu$m, and uniform electron distribution in the drain drift region is

$$\frac{I_d}{r_j W v_{sat}} = qN_A \tag{48}$$

i.e.,

$$\begin{aligned} I_d &= qN_A r_j W v_{sat} \\ &= 1.6 \times 10^{-19} \times 10^{16} \times (0.4 \times 10^{-4}) \times (1 \times 10^{-4}) \times 10^{7} \\ &= 64\ \mu\text{A}. \end{aligned}$$

For a typical driver, this range of current is quite common, so that the screening effect of the electron space charge on channel length modulation must be included in a correct model.

In the above example we have assumed that the electrons are uniformly distributed in the region beyond pinchoff. It is necessary, of course, to incorporate the fact that they are confined to the inversion layer of ~200 nm at the pinchoff point and fan out to the depth of the drain, depending on the ratio of the longitudinal to transverse field. The electron related space charge can then be represented by

$$Q_e = \frac{I_d}{[d + (r_j - d)\,(x/\Delta L)]\, w\, v_{sat}\, \eta} \tag{49}$$

where

d = depth of the inversion layer

L = the channel length modulation

η = E_x/E_y is the field spreading factor.

The estimates of E_v and E_y may be written simply as

$$E_v = \frac{V_{DS} - V_{DSAT}}{\sqrt{K\,(V_{DS} - V_{DSAT})}} \tag{50}$$

$$E_y = \frac{(V_{GS} - V_{to} + V_{BS} + V_{bi})}{\left[r_j + \sqrt{K\,(V_{DS} + V_{bs} + V_{bi})}\right]} \tag{51}$$

which then allows us to calculate the field spreading factor, which is assumed to be constant in the following calculation.

The channel length modulation is calculated from the solution of Poisson's equation

$$\frac{d^2V}{dx^2} = \frac{1}{\epsilon_s}(Q_e + qN_A) \tag{52}$$

with the boundary condition that

$$V(L) - V(L - \Delta L) = V_{DS} - V_{DSAT} \tag{53}$$

$$I_d = \frac{I_{DSAT}}{1 - (\Delta L/L)} \tag{54}$$

$$-\left(\frac{dV}{dx}\right)_{(L\ \ \Delta L)} = E_c \tag{55}$$

The solution to this equation is written as

$$\Delta L = \sqrt{\left[\frac{E_c}{2(qN_A/2\epsilon_s + Z)}\right]^2 + \frac{(V_{DS} - V_{DSAT})}{(qN_A/2\epsilon_s + Z)}} - \frac{E_c}{2(qN_A/2\epsilon_s + Z)} \tag{56}$$

where

$$Z = \frac{I_D}{2\epsilon\eta\, r_j\, w\, v_{sat}} \qquad \left(\log\frac{r_j}{d} - 1\right) \tag{57}$$

Equations (46) and (47) may be used simultaneously to calculate I_d and L. However, this procedure is not attractive for a CAD-oriented model because the solution becomes interactive. If, however, I_{DSAT} is substituted for I_D in Equation (46), then ΔL is directly computed, and channel length modulation may be incorporated.

F. SUBTHRESHOLD REGION

The modeling of subthreshold characteristics essentially follows the work of Taylor,[5] but uses the dynamic average doping transformation in the calculation of the charge-sharing factor. The surface potential using the charge-sharing factor may be calculated from the electrostatic gate-charge balance equation neglecting the inversion charge

$$\phi_S = V_{GS} - V_{FB} + V_o - \sqrt{(V_{GS} - V_{FB} + V_o)^2 - (V_{GS} - V_{FB})^2 + 2V_o V_{BS}} \tag{58}$$

[5]B.T. Murphy, "Unified Field-Effect Transistor Theory Including Velocity Saturation," *IEEE J. Solid State Circuits*, SC-15 (1980), p. 325.

where

$$V_o = q\epsilon_s N_A(V_{BS})\, F^2/C_o^2$$

The surface potential may be used to determine the electron density at the source boundary. The continuity equation may then be solved as shown in Reference 15 to obtain the subthreshold current equation.

$$I_d = \frac{W\{qD\overline{X}_d n_i\}\, e\, \frac{q(\phi_s - \phi_f)}{kT}}{L - \sqrt{K(V_{bi} - \phi_S)} - \sqrt{K(V_{bi} + V_{DS} - \phi_S)}} + \frac{\left(1 - e\, \frac{-q\, V_{DS}}{kT}\right)}{2\sqrt{\frac{\epsilon_S\, kT}{q^2\, N_A(V_{BS})}}} \tag{59}$$

In the above expression

$$\overline{x}_d = \sqrt{\epsilon_s \frac{kT}{2q^2} \overline{N}_A \left\{\left(\frac{q\phi_s}{kT}\right) + 1\right\}} \tag{60}$$

represents the effective channel depth available for free charge conduction at the Si/SiO_2 interface. The effective acceptor density includes the surface state density

$$N_A = \overline{N}_A + N_t\, kT \ln\left(\frac{n}{n_1}\right) \tag{61}$$

where N_t is the trap density located at energy E_1

$$n_1 = N_c \exp\left(\frac{E_1 - E_c}{kT}\right) \tag{62}$$

In practical short-channel devices, the acceptor density dominates the trap density, so that $N_A = \overline{N}_A$ and the depletion constant $k = 2\epsilon_s/q\overline{N}_A$.

In a model that describes the drain current continuously from subthreshold through the linear and saturation regions, it is very important to be able to match the current and conductance at the transition. This is accomplished by adding the subthreshold current calculated at $\phi_s = 2\phi_f$ to the above threshold current.[16]

G. SOURCE AND DRAIN RESISTANCE

In scaled devices with shallow source and drain regions, the sheet resistance of the n^+ silicon and contact resistance are quite important in determining gain. The feedback effects of these resistances were initially modeled by a mobility reduction

$$\mu(R_S, R_D) = \frac{\mu}{1 + \mu\, C_o \frac{W}{L} (V_{GS} - V_T)(R_D + R_S) - \mu\, C_o \frac{W}{L} R_D\, V_{DS}} \tag{63}$$

[16]H.G. Lee, S.Y. Oh, and G. Fuller, "A Simple and Accurate Method to Measure the Threshold Voltage of an Enhancement Mode MOSFET," *IEEE Trans. Electron Devices*, **ED-29** (1982), p. 346.

This method calculates the bulk charge, charge-sharing factor, and mobility reduction of velocity saturation using the applied voltages. When R_s and R_d are large, this assumption can introduce errors that can be avoided as discussed below. Also, adjustment to the terminal voltages means that V_{GS} and V_{BS} are varying during the calculation, which makes comparison to experimental data, (where the values are held constant) difficult.

Because of these problems, an iteration scheme is used in the charge-sharing program, allowing a self-consistent determination of the intrinsic device terminal voltages for a given set of applied terminal voltages. The program user has the capability of setting the accuracy to which the intrinsic terminal voltages are determined by use of the VERROR input.

H. COMPARISON WITH EXPERIMENTAL DATA

The current-voltage characteristics predicted by the charge-sharing model have been compared to measured data from devices fabricated using the process and structure assumed for the prediction. Figure 8 shows the comparison of the subthreshold region characteristics of an $L = 1.1$ μm MOSFET and the predicted characteristics on the basis of the charge-sharing model. The dependence of the subthreshold characteristics on the drain and substrate bias is well represented.

Figure 9(a), (b), and (c) show the predicted and measured characteristics of three MOSFETs fabricated in different laboratories using different processes. Figure 9(a) shows a MOSFET with an effective channel length of 1.1 μm and a gate oxide thickness of 50 nm and $N_{II} = 1.2 \times 10^{16}$ cm^{-3} fabricated to accentuate the short-channel effects. Figure 9(b) shows a MOSFET with an effective channel length of 1.1 μm and 39-nm gate oxide with a heavier doping ($N_{II} = 3.5 \times 10^{16}$ cm^{-3}). Figure 9(c) shows a MOSFET with an effective channel length of 0.8 μm and a gate oxide thickness of 35 nm and $N_{II} = 8 \times 10^{16}$ cm^{-3}. Notice that the predicted characteristics are remarkably close to the measured value, showing the validity of the device model.

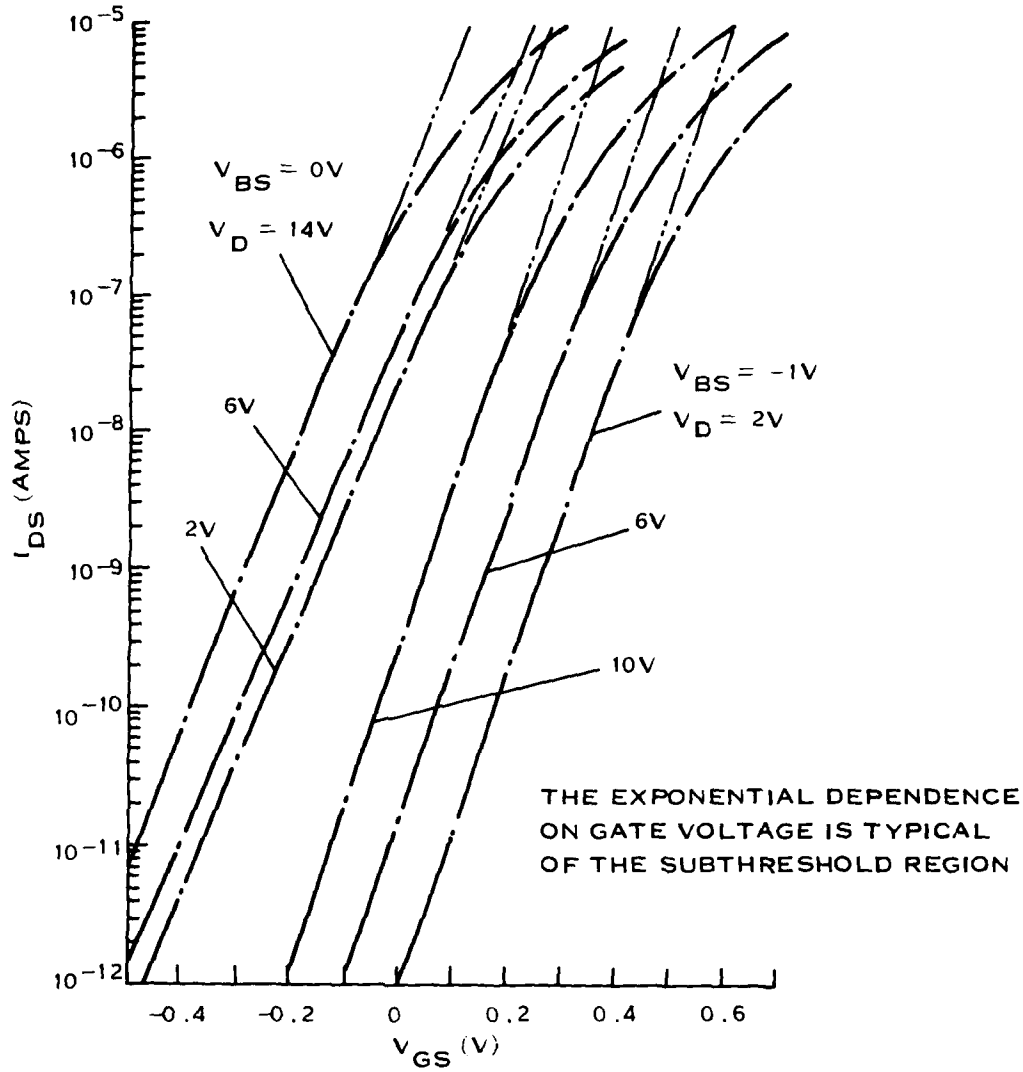
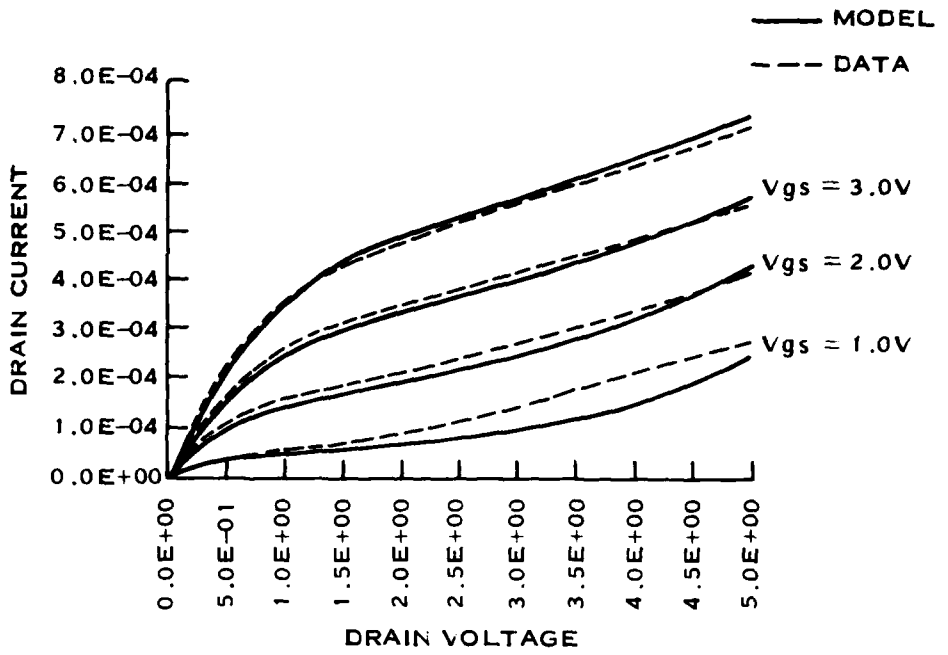
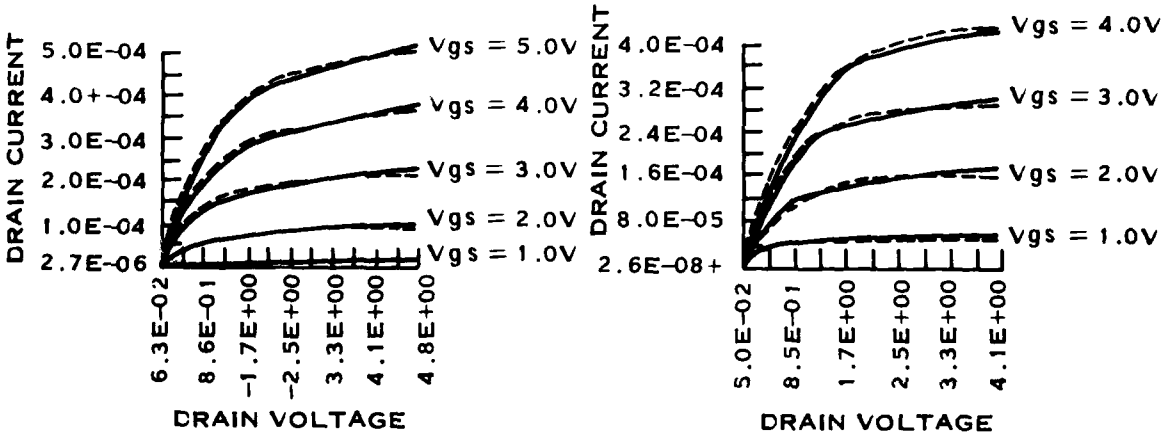


Figure 8. Variation of Subthreshold Current With Gate Voltage Having Drain Voltage as a Parameter



(A) t_{ox} = 50 NM Na = 1.2 X 10^{16} L = 1.1 μM



(B) t_{ox} = 39 NM Na = 3.5 X 10^{16}
L = 1.0 μM

(C) t_{ox} = 33 NM Na = 8.0 X 10^{16}
L = 0.8 μM

Figure 9. Calculated Versus Measured I-V Characteristics of Short-Channel Transistors

SECTION III

SILICON-ON-INSULATOR MOSFET MODEL

A. INTRODUCTION

An accurate long-channel MOSFET model dates as far back as 1966 when Pao and Sah[17] solved the exact continuity and charge neutrality equations along the length of a uniformly doped channel assuming constant mobility. The effect of normal field dependence of channel mobility on such devices has recently been incorporated.[18] However, most prevalent models use approximate surface potentials at source and drain, primarily for simplicity.[19-21] These models are of limited usefulness in predicting the weak inversion characteristics. Such models have also been used to assess the response of SOS and DI MOSFETs.[22-24] No model has been reported to predict the characteristics of practical SOI MOSFETs. The availability of an accurate SOI device model that can handle implanted substrate impurity distributions and that does justice to device physics is thought to be crucial at this stage.

A five-terminal physical device model for an inversion mode long and wide channel silicon-on-insulator MOSFET is presented. For concreteness, an n-channel device is analyzed; however, the model also holds good for a similar p-channel MOSFET. The device structure is shown in Figure 10, where various terminals and device dimensions are illustrated. To preserve generality, all terminals have been referred to a common external ground.

A step doping profile is assumed in the substrate to accommodate a low- and high-dose implant generally placed at the front and back interfaces, respectively, to independently adjust their threshold voltages. The idealized step profile of Figure 11 easily submits to an analytical treatment. This step profile is optimized to closely approximate the normal surface electric field as a function of surface potential obtained from the actual substrate impurity profile. This procedure, outlined in Appendix A, allows ease of formulation with least sacrifice in accuracy.

There are several practical reasons the bulk may not be degenerately doped. The electric field in this region does not vanish suddenly as in a metal gate. The effect of finite doping in the bulk is incorporated in the calculation of the back interface depletion depth. For analytical facility, the depletion approximation is invoked where applicable.

B. SUBSTRATE DOPING DENSITIES

For reproducibility, the parameters of the substrate must conform to the following requirements; however, the subsequent model transcends any such limitations and can be applied to other cases as well.

[17]H.C. Pao and C.T. Sah, *Solid State Electronics*, Vol. 9, pp. 927–937 (1966).
[18]D.H. Harper, Ph.D. Dissertation, Carleton University (1980).
[19]B. Hoeneisen and C.A. Mead, *IEEE Trans. Electron Dev.*, **ED-19** (1972), pp. 382–383.
[20]H.K.J. Ihantola, Stanford Electronics Laboratories Technical Report, No. 1661–1 (1961).
[21]P. Richman, MOS Field Effect Transistors and Integrated Circuits, Wiley (1973).
[22]E.P. Worley, *IEEE Trans. Electron Dev.*, **ED-24**, (1977) pp. 1342–1345.
[23]V. Kowshik and D.J. Dumin, *IEEE Trans. Electron Dev.*, **ED-28**, (1981), pp. 993–1002.
[24]P.W. Barth, Ph.D. Dissertation, Stanford University (1980).

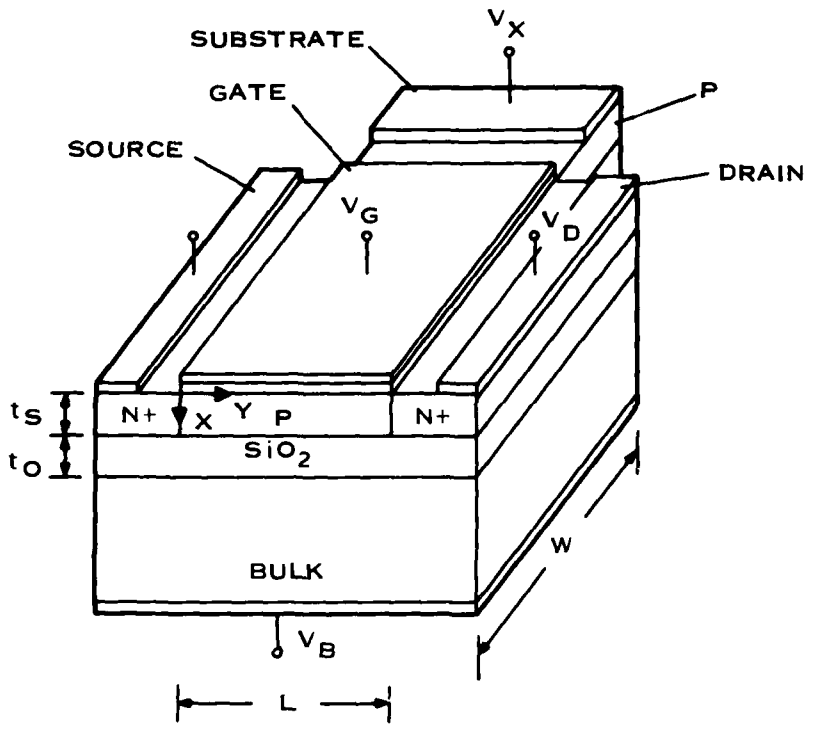
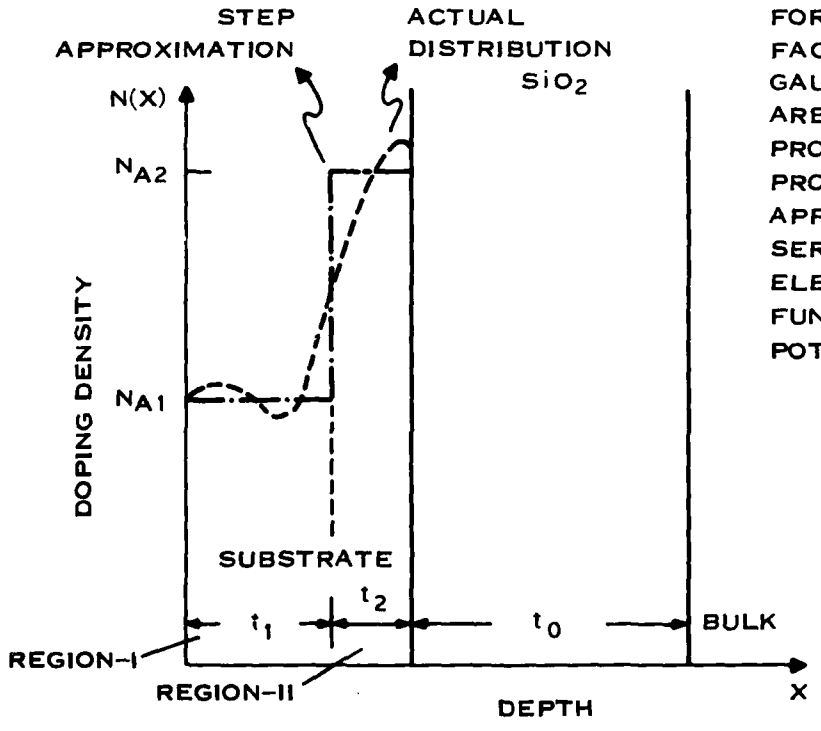


Figure 10. Schematic Cross Section of Five-Terminal SOI-MOSFET Analyzed, Illustrating Terminal Potential, Axis, and Dimension Designations



FOR ANALYTICAL FACILITY, THE IMPLANTED GAUSSIAN DISTRIBUTIONS ARE REDUCED TO A STEP PROFILE FOLLOWING THE PROCEDURE OUTLINED IN APPENDIX A THAT PRESERVES THE SURFACE ELECTRIC FIELD AS A FUNCTION OF SURFACE POTENTIAL

Figure 11. Idealized Step Doping Density of Two Regions in Substrate

The doping density of region I, N_{A1}, is chosen to yield the required threshold voltage.

The thickness of region I, t_1, must not be fully depleted at the turnon voltage for the surface channel.* It is shown in Appendix D that if the depletion layer, created by the gate at turnon, starts interacting with the substrate depleted by the effect of the bulk, the device threshold voltage becomes less controllable. This happens because, under the condition of space charge interaction, the depletion charge term in the threshold voltage develops dependence on various parameters that are normally not tightly controlled.

The doping density in region II, N_{A2}, is chosen to avoid back interface inversion in the presence of its fixed oxide charge. This doping density is sufficiently large even to prohibit weak inversion of the back interface.*

The thickness of region II, t_2, must accommodate the substrate depletion layer caused by the bulk effect.

C. MODEL EQUATIONS

1. Threshold Voltage

When the device design is conducted as suggested in Section II, the depletion region created by the gate at turnon does not interact with the substrate depletion layer caused by the bulk effect, and the threshold voltage of the device is given by the usual expression,

$$V_T = \frac{2\phi_{F1} + \phi_{GX} - Q_{f1}/C_o + \{2\epsilon_s qN_{A1} \cdot (V_S + 2\phi_{F1} - V_X)\}^{1/2}}{C_o + V_S} \tag{64}$$

where

V_T = gate voltage at turnon

V_S, V_X = source and substrate voltages, respectively

ϕ_{GX} = gate-to-substrate work function difference

N_{A1}, ϕ_{F1} = doping density and Fermi potential, respectively, of region I in the substrate

Q_{f1} = effective fixed charge density at the gate oxide-substrate interface

C_o = gate oxide capacitance

q = electronic charge

ϵ_s = permittivity of silicon.

In case the space charge interaction between the depletion layers created at both interfaces occurs at turnon, the threshold voltage is no longer given by Equation (64). The threshold voltage calculation for this case is given in Appendix D. The threshold voltage expression is reproduced here,

$$V_T = \left[V_S + 2\phi_{F1} + \phi_{GX} - \frac{Q_{f1}}{C_o} - \frac{q}{C_o}(N_{A2} - N_{A1})\, t_1 + \frac{C_c}{C_o}\left\{ \frac{q}{2\epsilon_s}(N_{A2} - N_{A1})\, t_1^2 \right.\right.$$

$$\left. + \frac{q}{C_o}(N_{A2} - N_{A1})\, t_1 + qN_{A2}\, t_s\left(\frac{1}{2C_s} + \frac{1}{C_{ob}}\right) - \left(\phi_{GX} - \frac{Q_{f1}}{C_o}\right) - V_B + \phi_b \right. \tag{65}$$

$$\left.\left. + \left(\phi_{BX} - \frac{Q_{f2}}{C_{ob}}\right)\right\}\right] \Big/ \left(1 - \frac{C_c}{C_o}\right)$$

*For grounded bulk, substrate, and source.

where

$$Q_s = qN_{A1}t_1 + qN_{A2}t_2$$

$$C_s = \frac{\epsilon_s}{t_s}$$

$$C_{ob} = \frac{\epsilon_o}{t_o}$$

$$C_c = \left(\frac{1}{C_s} + \frac{1}{C_{ob}} + \frac{1}{C_o}\right)^{-1}$$

In Equation (65), the threshold voltage depends on the parameters of the buried oxide (C_{ob}, Q_{f2}), region II in the substrate (N_{A2}, ϕ_{BX}, t_2), and the total substrate thickness (t_s, C_s) in addition to other usual parameters. As an example, Figure 12 shows V_T as a function of t_2 and N_{A2} for a typical case. It is seen that the device threshold voltage is fairly sensitive to variations in either of these parameters. Furthermore, the threshold voltage is smaller than the value without space charge interaction.

The threshold voltage sensitivity can be improved vastly if the device design prevents space charge interaction until after the device turnon voltage. Such a design philosophy has been outlined in Section II. Figure 13 presents the plot of interrelationship between Q_{f2}, N_{A2}, t_2, and N_{A1}, t_1, which permits a device design that avoids back interface inversion and space charge interaction before turnon.

2. Drain Current Formulation

The drain current of the device can be expressed as

$$I_D = \mu W \cdot \left(Q_m - \frac{kT}{q} \cdot \frac{\partial Q_m}{\partial \phi_s}\right) \cdot \frac{\partial \phi_s}{\partial y} \tag{66}$$

where

μ, Q_m, ϕ_s = channel mobility, mobile channel charge density, and surface potential, respectively, at a distance y from the source

k = Boltzmann constant

T = absolute temperature

W = channel width.

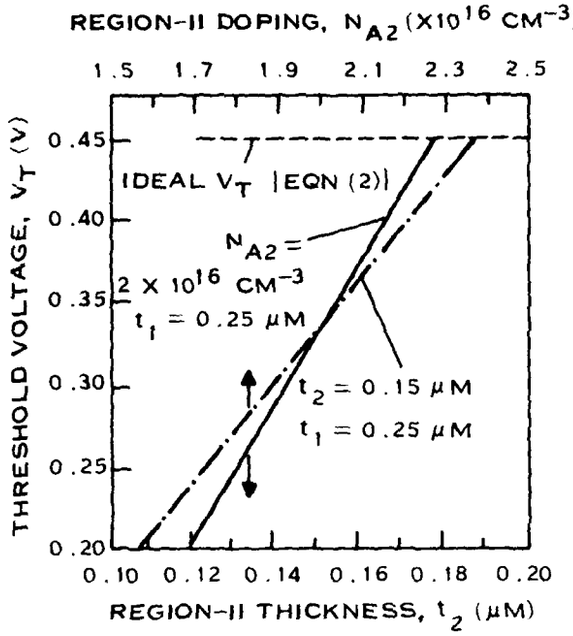
The above expression for drain current includes both drift and diffusion current components permitting drain current determination from weak inversion to strong inversion.

For a long-channel device, lateral channel field is small enough not to affect channel mobility. However, the normal field cannot be ignored. The effect of varying normal field along the channel can be effectively modeled as[25,18]

$$\mu = \frac{\mu_0}{\left(1 + \frac{V_g - \phi_s}{V_c}\right)} \tag{67}$$

where μ_0 is the zero field mobility, V_g is the effective gate voltage ($V_g = V_G - \phi_{GX} + Q_{fi}/C_o$), and V_c is a device constant ($V_c = E_c \epsilon_s / C_o$, $E_c \simeq 10^4$ V/cm).

[25]A.G. Sabnis and J.T. Clemens, IEDM Tech. Digest (1977).



IF SPACE CHARGE INTERACTION BETWEEN THE GATE AND BULK TERMINALS OCCURS BEFORE DEVICE TURNON, THE DEVICE THRESHOLD VOLTAGE BECOMES A SENSITIVE FUNCTION OF BACK CHANNEL IMPLANT PARAMETERS. A DEVICE DESIGNED TO PRECLUDE SUCH INTERACTION UNTIL AFTER DEVICE TURNON HAS A V_T INDEPENDENT OF N_{A2} AND t_2.

$N_{A1} \approx 1 \times 10^{16}\ CM^{-3}$

$Q_{f1} \approx 3 \times 10^{-9}\ C.CM^{-2}$

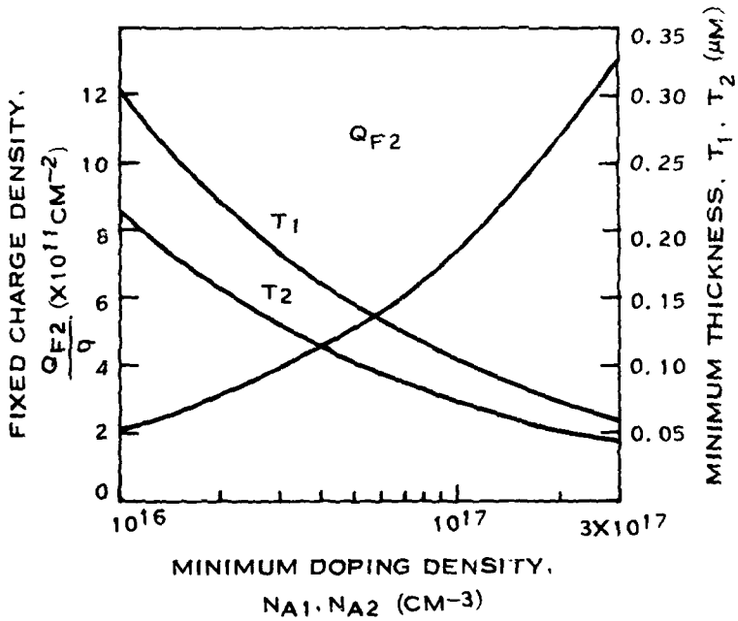
$Q_{f2} \approx 5 \times 10^{-8}\ C.CM^{-2}$

$C_o \approx 6.94 \times 10^{-8}\ f.CM^{-2}$

$t_o \approx 1\ \mu M$

$V_S \approx V_X \approx V_B = 0V$

Figure 12. Threshold Voltage Typically Sensitive to Doping and Total Thickness



FOR REPRODUCIBLE THRESHOLD VOLTAGE, THE DEVICE SHOULD BE DESIGNED TO PROHIBIT SPACE CHARGE INTERACTION UNTIL AFTER DEVICE TURN ON.

Figure 13. Doping Density Versus Back Interface Fixed Charge Density and Thickness for Reproducible Threshold Voltage

Equation (67) differs significantly from mobility expressions in other analytical models[26] that try to capture the normal field mobility reduction mechanism by

$$\mu = \frac{\mu_0}{\left(1 + \frac{V_G - V_T}{V_c}\right)} \tag{68}$$

The use of Equation (68) entails a considerable simplification of the subsequent integration but fails to truly represent the normal field along the channel. For example, it overestimates the normal field near the drain end, thereby underestimating the channel mobility. In the present formulation, the rigor of Equation (67) is intentionally adopted to achieve accuracy.[2]

The mobile channel charge density can be expressed as

$$Q_m = C_o (V_g - \phi_s) - Q_D \tag{69}$$

where Q_D is the depletion charge density.

Using Equations (67) and (69) in Equation (66),

$$I_D = \mu_0 C_o \frac{W}{L} \int_{\phi_{SS}}^{\phi_{SD}} \left\{ \frac{(V_g - \phi_s) - Q_D/C_o}{1 + \frac{V_g - \phi_s}{V_c}} + \frac{kT}{q} \cdot \frac{1 + \frac{1}{C_o}\frac{\partial Q_D}{\partial \phi_s}}{1 + \frac{V_g - \phi_s}{V_c}} \right\} d\phi_s \tag{70}$$

where ϕ_{SS} and ϕ_{SD} are the surface potentials at source and drain, respectively.

The expression for depletion charge, Q_D, takes on different forms, depending on whether the depletion layer created by the gate is confined to region I or extends to region II and whether or not it interacts with the depletion charge associated with the bulk terminal. This leads to various expressions in drain current as discussed below in detail.

a. Channel Depletion Layer Confined to Region I

At small gate and drain voltages, the surface potential throughout the channel may confine the resultant depletion region to region I. The cross section of the device under such bias conditions is shown in Figure 14. From the solution of a one-dimensional Poisson equation, the depletion depth and the charge density can be expressed as

$$x_D(y) = \left[\frac{2\epsilon_s}{qN_{A1}} \{\phi_s(y) - V_X\} \right]^{1/2} \tag{71}$$

$$Q_D(y) = [2\epsilon_s qN_{A1} \{\phi_s(y) - V_X\}]^{1/2} \tag{72}$$

Equations (71) and (72) remain valid as long as region I is not fully depleted, or

$$\phi_s(y) \leq \frac{qN_{A1} t_1^2}{2\epsilon_s} + V_X = \phi_1 \tag{73}$$

Putting Equation (72) in Equation (70) and integrating,

[26]L.M. Dang, IEEE Trans. Electron Dev., ED-26, 1979, pp. 436–445.

$$I_D = \mu_0 C_o \frac{W}{L}\left[V_c(\phi_{SD} - \phi_{SS}) + (2\epsilon_s qN_{A1})^{1/2} \cdot \frac{2V_c}{C_o}\{(\phi_{SD} - V_X)^{1/2} - (\phi_{SS} - V_X)^{1/2}\}\right.$$

$$- \left(V_c^2 - \frac{kT}{q} \cdot V_c\right) \ln \frac{V_c + V_g - \phi_{SS}}{V_c + V_g - \phi_{SD}} - \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o} \tag{74}$$

$$\left\{V_c(V_c + V_g - V_X)^{1/2} - \frac{kT}{2q} \cdot \frac{V_c}{(V_c + V_g - V_X)^{1/2}}\right\}$$

$$\left. \cdot \ln \frac{(V_c + V_g - V_X)^{1/2} + (\phi_{SD} - V_X)^{1/2}}{(V_c + V_g - V_X)^{1/2} + (\phi_{SS} - V_X)^{1/2}} \cdot \frac{(V_c + V_g - V_X)^{1/2} - (\phi_{SS} - V_X)^{1/2}}{(V_c + V_g - V_X)^{1/2} - (\phi_{SD} - V_X)^{1/2}}\right]$$

The above equation can also be used to predict the drain current characteristics of a uniformly doped bulk device.

b. Channel Depletion Layer Extending to Region II

When the drain and gate voltages are increased further so that the surface potential on the drain end of the channel exceeds ϕ_t, region I gets fully depleted near the drain and the depletion region extends to region II. The schematic diagram of the device cross section is shown in Figure 15. The calculation of the depletion depth and the depletion charge density is given in Appendix B. The result is

$$x_D(y) = \left[\frac{2\epsilon_s}{qN_{A2}}\left\{\phi_s(y) - V_X - \frac{qN_{A1}\,t_1^2}{2\epsilon_s}\right\} + t_1^2\right]^{1/2} \tag{75}$$

$$Q_D(y) = [2\epsilon_s qN_{A2}\{\phi_s(y) + \phi_A\}]^{1/2} - qt_1(N_{A2} - N_{A1}) \tag{76}$$

where

$$\phi_A = \frac{q}{2\epsilon_s}(N_{A2} - N_{A1})\,t_1^2 - V_X$$

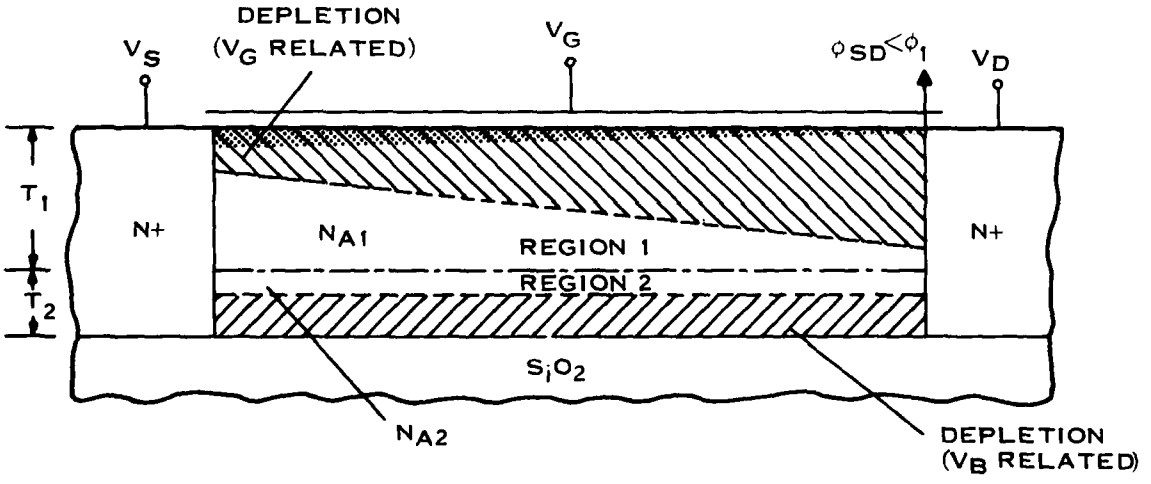


Figure 14. Schematic Cross Section of Device When Channel Depletion Layer is Confined to Region 1

This condition persists as long as the channel depletion layer does not interact with the depletion charge associated with the bulk, or in terms of the surface potential

$$\phi_s(y) \leq \frac{qN_{A2}}{2\epsilon_s}(x_j^2 - t_1^2) + \frac{qN_{A1}}{2\epsilon_s}t_1^2 + V_X = \phi_t \tag{77}$$

where x_j is the location of the depletion layer associated with the bulk terminal and is derived in Appendix C to be

$$x_j = t_1 + \frac{\epsilon_s}{C_{ob}} - \left\{\left(\frac{\epsilon_s}{C_{ob}}\right)^2 + \frac{2\epsilon_s}{qN_{A2}}\left(V_B - V_X - \phi_b + \frac{Q_{f2}}{C_{ob}}\right)\right\}^{1/2} \tag{78}$$

The use of Equations (72) and (76) in Equation (70) yields

$$\begin{aligned} I_D = \mu_0 C_o \frac{W}{L}\Bigg[& V_c(\phi_{SD} - \phi_{SS}) + (2\epsilon_s qN_{A1})^{1/2}\frac{2V_c}{C_o}\{(\phi_1 - V_X)^{1/2} - (\phi_{SS} - V_X)^{1/2}\} \\ & + (2\epsilon_s qN_{A2})^{1/2}\frac{2V_c}{C_o}\{(\phi_{SD} + \phi_A)^{1/2} - (\phi_1 + \phi_A)^{1/2}\} - \left(V_c^2 - \frac{kT}{q}V_c\right)\ln\frac{V_c + V_g - \phi_{SS}}{V_c + V_g - \phi_{SD}} \\ & - \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o}\left\{V_c \cdot (V_c + V_g - V_X)^{1/2} - \frac{kT}{2q}\cdot\frac{V_c}{(V_c + V_g - V_X)^{1/2}}\right\} \\ & \cdot \ln\frac{(V_c + V_g - V_X)^{1/2} + (\phi_1 - V_X)^{1/2}}{(V_c + V_g - V_X)^{1/2} + (\phi_{SS} - V_X)^{1/2}} \cdot \frac{(V_c + V_g - V_X)^{1/2} - (\phi_{SS} - V_X)^{1/2}}{(V_c + V_g - V_X)^{1/2} - (\phi_1 - V_X)^{1/2}} \\ & - \frac{(2\epsilon_s qN_{A2})^{1/2}}{C_o}\left\{V_c(V_c + V_g + \phi_A)^{1/2} - \frac{kT}{2q}\frac{V_c}{(V_c + V_g + \phi_A)^{1/2}}\right\} \\ & \cdot \ln\frac{(V_c + V_g + \phi_A)^{1/2} + (\phi_{SD} + \phi_A)^{1/2}}{(V_c + V_g + \phi_A)^{1/2} + (\phi_1 + \phi_A)^{1/2}} \cdot \frac{(V_c + V_g + \phi_A)^{1/2} - (\phi_1 + \phi_A)^{1/2}}{(V_c + V_g + \phi_A)^{1/2} - (\phi_{SD} + \phi_A)^{1/2}} \\ & + q(N_{A2} - N_{A1})t_1\frac{V_c}{C_o}\ln\frac{V_c + V_g - \phi_1}{V_c + V_g - \phi_{SD}}\Bigg] \end{aligned} \tag{79}$$

Equation (79) can also be used to predict the I-V characteristics of an implanted substrate bulk MOSFET.

c. *Channel Depletion Layer Interacts With Back Interface Depletion Charge*

On further increase in applied voltages, the surface potential on the drain side of the device would rise above ϕ_t. In such a situation, the space charge interaction ensues between the depletion charges associated with the gate and the bulk terminals. This is schematically shown in Figure 16. Appendix E gives the depletion depth and the charge density associated with the gate terminal as

$$x_D(y) = \{\phi_s(y) + \phi_B\} \cdot \frac{C_m}{qN_{A2}} \tag{80}$$

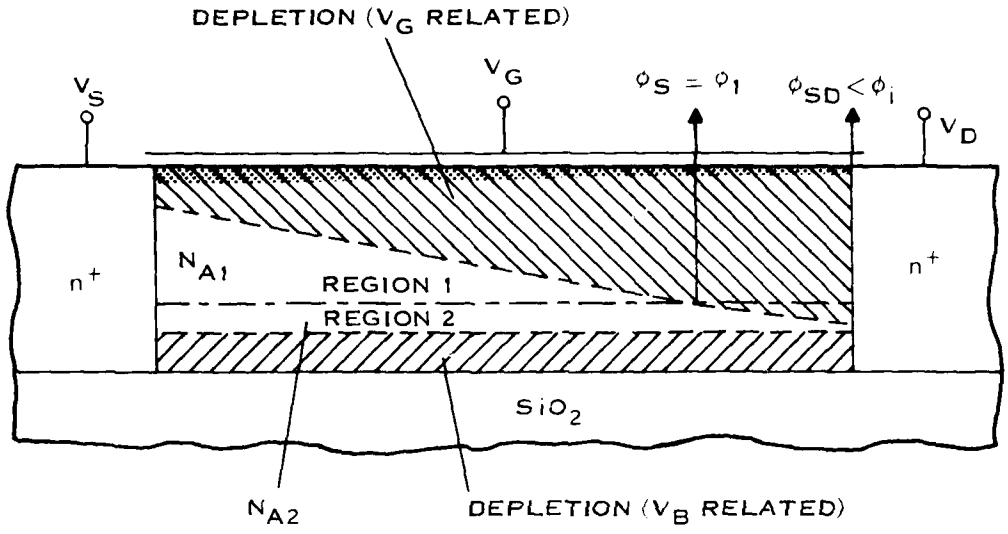


Figure 15. Schematic Cross Section of Channel Depletion Layer Extending Into Region 11 With Larger Applied Bias

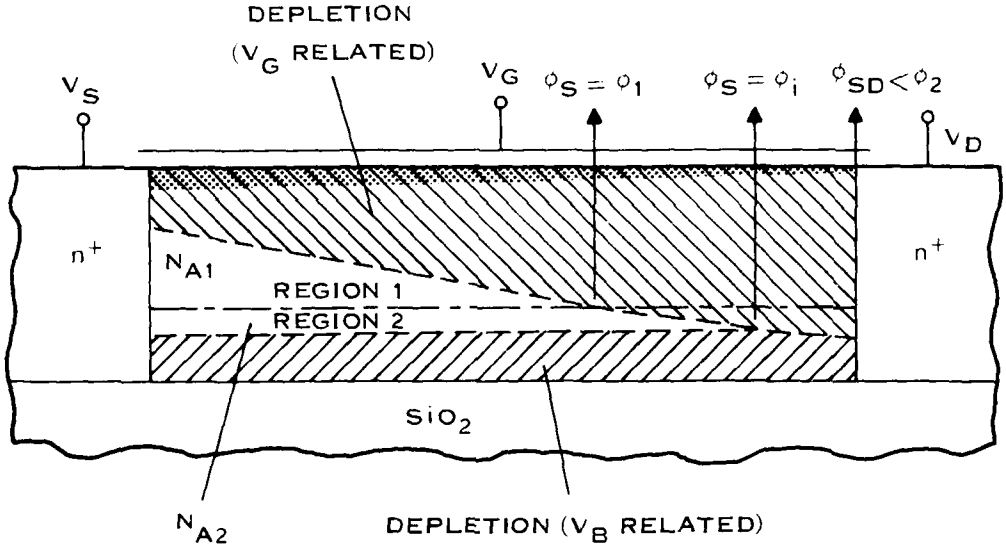


Figure 16. Schematic Cross Section of Device When the Channel Depletion Layer Undergoes Space Change Interaction With Back Interfce Depletion Layer Related to the Bulk Terminal

$$Q_D(y) = \phi_s C_m + Q_{D1} \tag{81}$$

where

$$C_m = \left(\frac{1}{C_{ob}} + \frac{1}{C_s}\right)^{-1}$$

$$\phi_B = \frac{q}{2\epsilon_s}(N_{A2} - N_{A1})t_1^2 + \frac{qN_{A2}\,t_s}{2\epsilon_s} + \frac{qN_{A2}}{C_{ob}}t_s + \phi_{BX} - \frac{Q_{I2}}{C_{ob}} - \phi_b - V_B$$

$$Q_{D1} = \phi_B C_m - q(N_{A2} - N_{A1})\,t_1$$

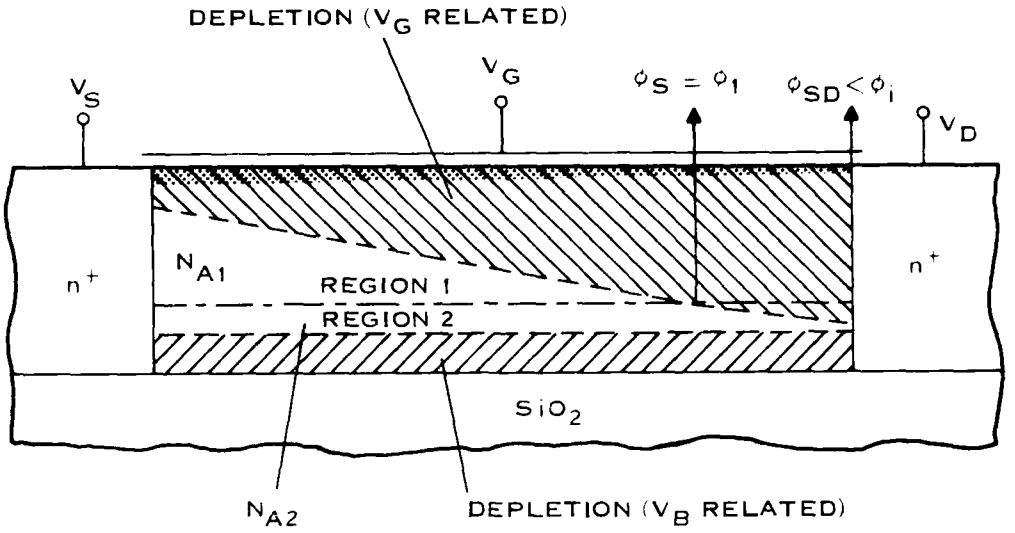


Figure 15. Schematic Cross Section of Channel Depletion Layer Extending Into Region 11 With Larger Applied Bias

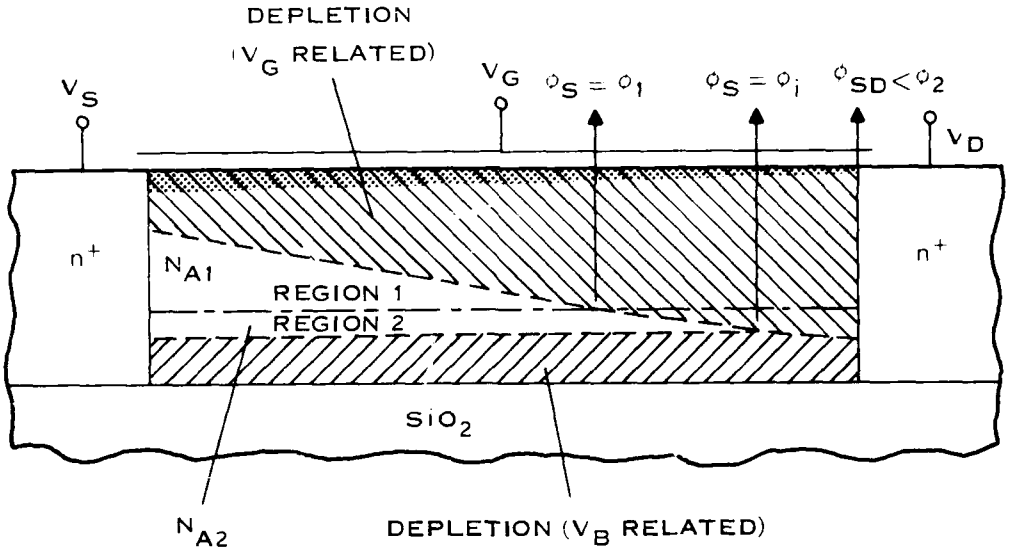


Figure 16. Schematic Cross Section of Device When the Channel Depletion Layer Undergoes Space Change Interaction With Back Interfce Depletion Layer Related to the Bulk Terminal

$$Q_D(y) = \phi_s C_m + Q_{Di} \tag{81}$$

where

$$C_m = \left(\frac{1}{C_{ob}} + \frac{1}{C_s}\right)^{-1}$$

$$\phi_B = \frac{q}{2\epsilon_s}(N_{A2} - N_{A1})t_1^2 + \frac{qN_{A2}\,t_s}{2\epsilon_s} + \frac{qN_{A2}}{C_{ob}}t_s + \phi_{BX} - \frac{Q_{f2}}{C_{ob}} - \phi_b - V_B$$

$$Q_{Di} = \phi_B C_m - q(N_{A2} - N_{A1})\,t_1$$

This condition would persist as long as

$$\phi_s(y) \leq \frac{Q_s - Q_{D_t}}{C_m} = \phi_2 \tag{82}$$

Using Equations (72), (76), and (81) in Equation (70),

$$\begin{aligned} I_D = \mu_0 C_o \frac{W}{L} \Bigg[& V_c(\phi_{SD} - \phi_{SS}) + (2\epsilon_s qN_{A1})^{1/2} \cdot \frac{2V_c}{C_o} \{(\phi_1 - V_X)^{1/2} - (\phi_{SS} - V_X)^{1/2}\} \\ & + (2\epsilon_s qN_{A2})^{1/2} \cdot \frac{2V_c}{C_o} \{(\phi_t + \phi_A)^{1/2} - (\phi_1 + \phi_A)^{1/2}\} - \left(V_c^2 - \frac{kT}{q} \cdot V_c\right) \\ & \cdot \ln \frac{V_c + V_g - \phi_{SS}}{V_c + V_g - \phi_{SD}} - \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o} \left\{ V_c (V_c + V_g - V_X)^{1/2} - \frac{kT}{2q} \cdot \frac{V_c}{(V_c + V_g - V_X)^{1/2}} \right\} \\ & \cdot \ln \frac{(V_c + V_g - V_X)^{1/2} + (\phi_1 - V_X)^{1/2}}{(V_c + V_g - V_X)^{1/2} + (\phi_{SS} - V_X)^{1/2}} \cdot \frac{(V_c + V_g - V_X)^{1/2} - (\phi_{SS} - V_X)^{1/2}}{(V_c + V_g - V_X)^{1/2} - (\phi_1 - V_X)^{1/2}} \\ & - \frac{(2\epsilon_s qN_{A2})^{1/2}}{C_o} \left\{ V_c (V_c + V_g + \phi_A)^{1/2} - \frac{kT}{2q} \frac{V_c}{(V_c + V_g + \phi_A)^{1/2}} \right\} \\ & \cdot \ln \frac{(V_c + V_g + \phi_A)^{1/2} + (\phi_t + \phi_A)^{1/2}}{(V_c + V_g + \phi_A)^{1/2} + (\phi_1 + \phi_A)^{1/2}} \cdot \frac{(V_c + V_g + \phi_A)^{1/2} - (\phi_1 + \phi_A)^{1/2}}{(V_c + V_g + \phi_A)^{1/2} - (\phi_t + \phi_A)^{1/2}} \\ & + q(N_{A2} - N_{A1})\, t_1 \frac{V_c}{C_o} \cdot \ln \frac{V_c + V_g - \phi_1}{V_c + V_g - \phi_t} - \frac{C_m}{C_o} V_c \left(V_c + V_g + \frac{Q_{D_t}}{C_m} - \frac{kT}{q} \right) \\ & \cdot \ln \frac{V_c + V_g - \phi_t}{V_c + V_g - \phi_{SD}} + \frac{C_m}{C_o} V_c \cdot (\phi_{SD} - \phi_t) \Bigg] \end{aligned} \tag{83}$$

d. Channel Depletion Layer Exhausts the Substrate

As the applied voltages are increased, the space charge interaction becomes stronger. At sufficiently large drain and gate bias, the total substrate depletion charge communicates with the gate terminal, as shown in Figure 17.

This condition occurs when

$$\phi_s(y) \geq \frac{Q_s - Q_{D_t}}{C_m} \tag{84}$$

Now the depletion depth and charge density are given by

$$x_D(y) = t_s \tag{85}$$

$$Q_D(y) = q(N_{A1}\, t_1 + N_{A2}\, t_2) = Q_s \tag{86}$$

The drain current of the device as given by Equations (72), (76), (81), (86) and (70) can be written as

$$
\begin{aligned}
I_D = \mu_0 C_o \frac{W}{L}\Bigg[& V_c(\phi_{SD} - \phi_{SS}) + (2\epsilon_s qN_{A1})^{1/2} \cdot \frac{2V_c}{C_o} \\
& \cdot \{(\phi_1 - V_X)^{1/2} - (\phi_{SS} - V_X)^{1/2}\} + (2\epsilon_s qN_{A2})^{1/2} \cdot \frac{2V_c}{C_o}\{(\phi_t + \phi_A)^{1/2} - (\phi_1 + \phi_A)^{1/2}\} \\
& - \left(V_c^2 - \frac{kT}{q} \cdot V_c\right) \cdot \ln \frac{V_c + V_g - \phi_{SS}}{V_c + V_g - \phi_{SD}} \\
& - \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o}\left\{V_c(V_c + V_g - V_X)^{1/2} - \frac{kT}{2q} \cdot \frac{V_c}{(V_c + V_g - V_X)^{1/2}}\right\} \\
& \cdot \ln \frac{(V_c + V_g - V_X)^{1/2} + (\phi_1 - V_X)^{1/2}}{(V_c + V_g - V_X)^{1/2} - (\phi_{SS} - V_X)^{1/2}} \cdot \frac{(V_c + V_g - V_X)^{1/2} + (\phi_{SS} - V_X)^{1/2}}{(V_c + V_g - V_X)^{1/2} - (\phi_1 - V_X)^{1/2}} \\
& - \frac{(2\epsilon_s qN_{A2})^{1/2}}{C_o}\left\{V_c(V_c + V_g + \phi_A)^{1/2} - \frac{kT}{2q} \cdot \frac{V_c}{(V_c + V_g + \phi_A)^{1/2}}\right\} \\
& \cdot \ln \frac{(V_c + V_g + \phi_A)^{1/2} + (\phi_t + \phi_A)^{1/2}}{(V_c + V_g + \phi_A)^{1/2} + (\phi_1 + \phi_A)^{1/2}} \cdot \frac{(V_c + V_g + \phi_A)^{1/2} - (\phi_1 + \phi_A)^{1/2}}{(V_c + V_g + \phi_A)^{1/2} - (\phi_t + \phi_A)^{1/2}} \\
& + q(N_{A2} - N_{A1})\, t_1 \cdot \frac{V_c}{C_o} \cdot \ln \frac{V_c + V_g - \phi_1}{V_c + V_g - \phi_t} - \frac{C_m}{C_o} V_c \left(V_c + V_g + \frac{Q_{D1}}{C_m} - \frac{kT}{q}\right) \\
& \cdot \ln \frac{V_c + V_g - \phi_t}{V_c + V_g - \phi_2} + \frac{C_m}{C_o} \cdot V_c(\phi_2 - \phi_1) - V_c \frac{Q_s}{C_o} \ln \frac{V_c + V_g - \phi_2}{V_c + V_g - \phi_{SD}}\Bigg]
\end{aligned}
\tag{87}
$$

Equations (74), (79), (83), and (87) give a detailed description of the drain current of the SOI MOSFET in its various regimes of operation. Furthermore, these expressions are valid from weak inversion to strong inversion and from presaturation to postsaturation.

To gain some perception of the effect of space charge interaction on the depletion charge, a plot of Q_D versus ϕ_s for a typical case is shown in Figure 18. It is observed that the space charge interaction slows down the increase in Q_D with ϕ_s. At large ϕ_s, the substrate is exhausted and Q_D attains a limiting value, Q_s. This has important implications for the electrical characteristics of the device as elaborated in the subsequent sections.

D. RESULTS AND DISCUSSION

1. SOI Device Model Comparison

Experimental data from n-channel silicon-on-insulator MOSFETs fabricated on unseeded laser-recrystallized material was used. These devices were fabricated in an n^+ polysilicon self-aligned technology using a complete isolation etch scheme. These devices did not have a substrate contact. The experimental

AT THE DRAIN END, THE FULLY DEPLETED SUBSTRATE CHARGE IS ASSOCIATED WITH THE GATE TERMINAL (TERMED AS THE SUBSTRATE EXHAUSTION EFFECT)

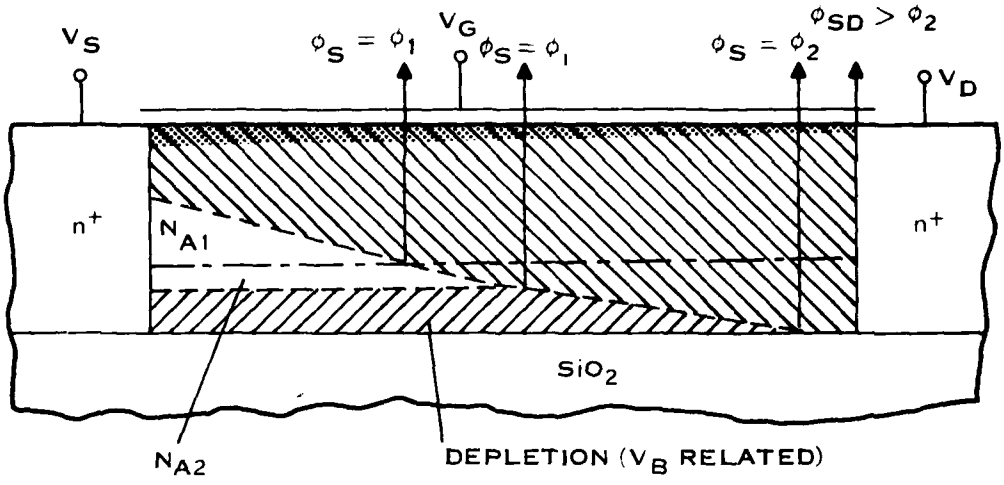


Figure 17. Schematic Cross Section for Large Applied Voltages and Strong Space Charge Intersection

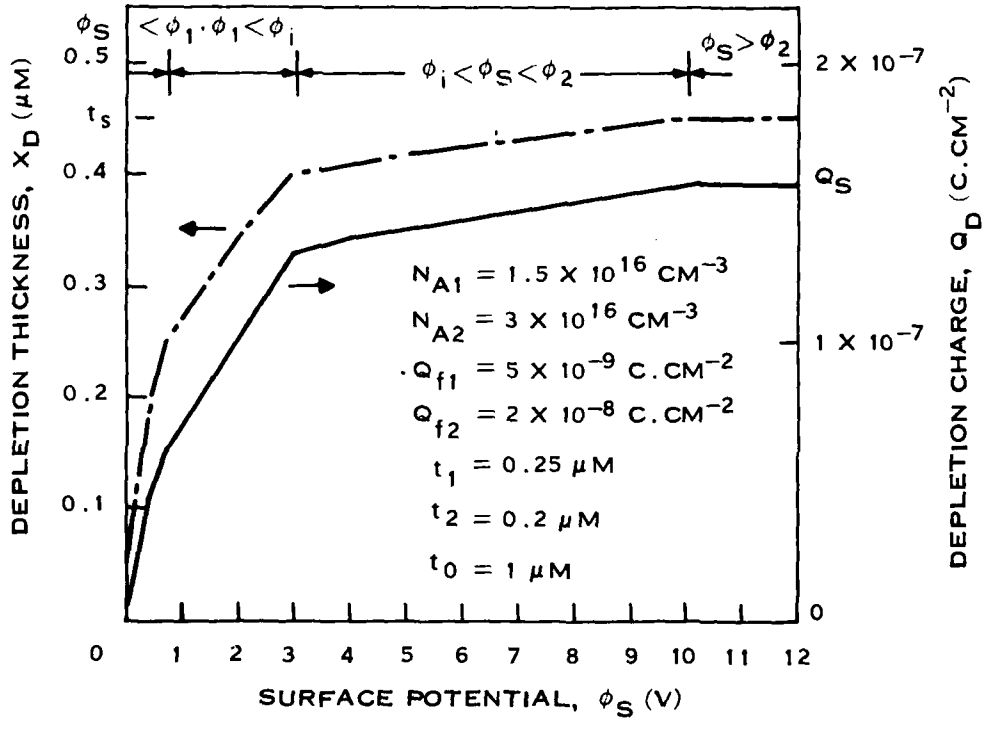


Figure 18. Channel Depletion Layer Thickness and Depletion Charge Density Versus Surface Potential for Typical Set of Parameters

data was obtained on an HP 9845B based data acquisition system. The source terminal was grounded. The device parameters as obtained from the fabrication schedule and model comparison are listed in Table 1.

TABLE 1. SUMMARY OF N-CHANNEL SOI MOSFET PARAMETERS

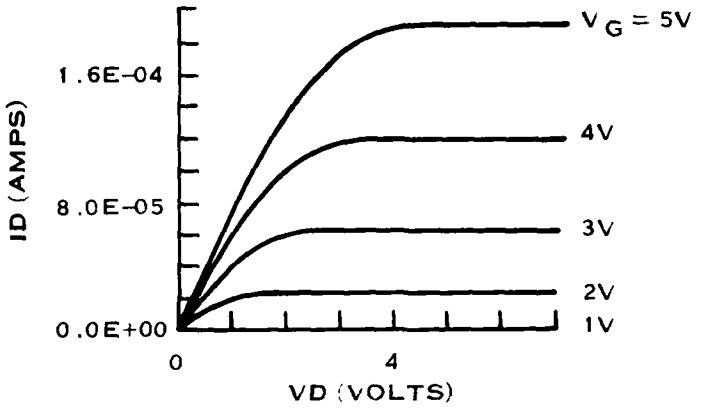
Parameter	Value
W	40 μm
L	40 μm
x_o	550 nm
t_s	4750 nm
t_o	1.1 μm
N_{A1}, N_{A2}	1.26×10^{16} cm^{-3}
N_{Ab}	2.5×10^{15} cm^{-3}
Q_{f1}	5×10^{-9} C cm^{-2}
Q_{f2}	5×10^{-8} C cm^{-2}
V_c	13 V
μ_0	425 cm^2 V^{-1} s^{-1}

The predicted I-V characteristics of the device with grounded bulk are shown in Figure 19(a). The measured characteristics superposed with this predicted data, in Figure 19(b), show good agreement. The predicted presaturation I_D versus V_G and postsaturation square root of I_D versus V_G characteristics also exhibit a close correspondence, as shown in Figure 20. The slope of the presaturation I_D versus V_G characteristics falls off at higher gate voltages, which is indicative of the mobility reduction at larger normal electric fields. A close examination of the postsaturation square root of I_D versus V_G curve reveals that its slope increases at larger gate voltages, a natural consequence of an SOI device featuring space charge interaction or substrate exhaustion. This observation is contrary to the bulk MOSFET response and is explained in detail in Subsection III.D.3 where it is tapped to make an important claim. This effect can be accentuated and, given the same material quality and threshold voltage, an SOI device can be designed to deliver a significantly larger drain current than a bulk device.

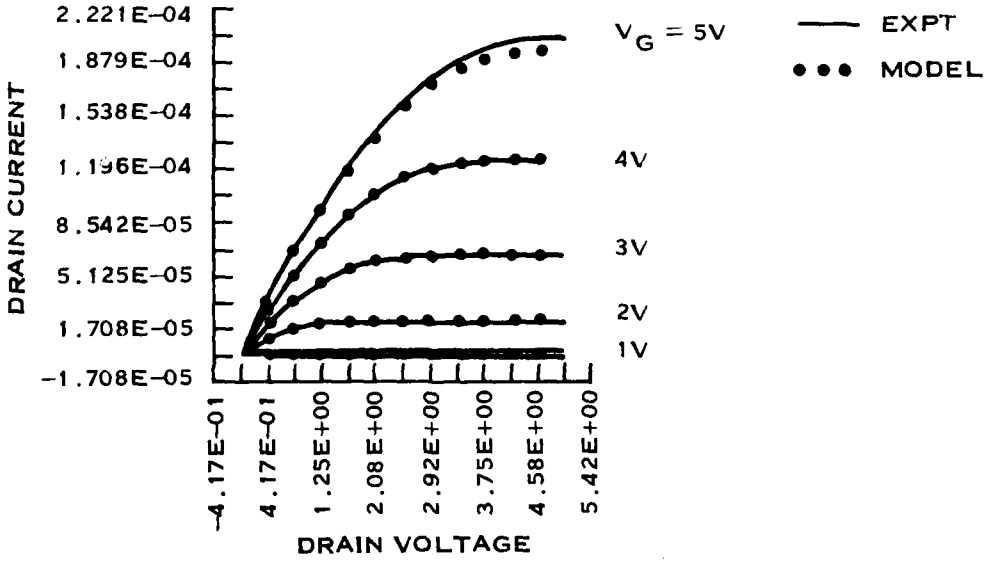
As shown in Figure 21, the experimental weak inversion does not agree with the model prediction. The cause for this disagreement can be traced to the parasitic conduction effects that may originate at the sidewalls resulting from complete isolation etch scheme.[27,28] Having poor electrical quality, the sidewall dielectric is characterized by lower threshold voltage than in the parent device. The sidewalls continue to conduct current well below the gate voltage where the parent device has shut off. No effort has been made to model this parasitic response because it can be eliminated in an improved process.

Next, the predicted I-V characteristics of the device with $V_B = -40$ V are shown in Figure 22(a). Again, the measured characteristics of the device superposed with the predicted data show an excellent agreement as in Figure 22(b). A comparison between Figures 19(a) and 22(a) discloses that the effect of the negative bias on the bulk is to reduce the drain current of the device. The outcome is peculiar to an SOI device, which involves space charge interaction between the depletion regions associated with the gate and the bulk terminals.

[27]A. Gupta et al., IEDM Tech. Digest (1981).
[28]Y.M. Chi et al., Device Research Conf. (1981).

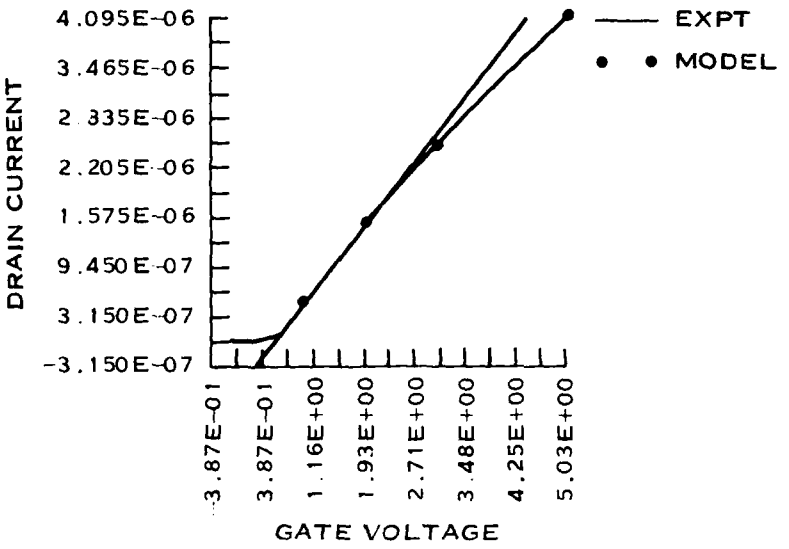


(A) PREDICTED I-V CHARACTERISTICS OF SOI-MOSFET

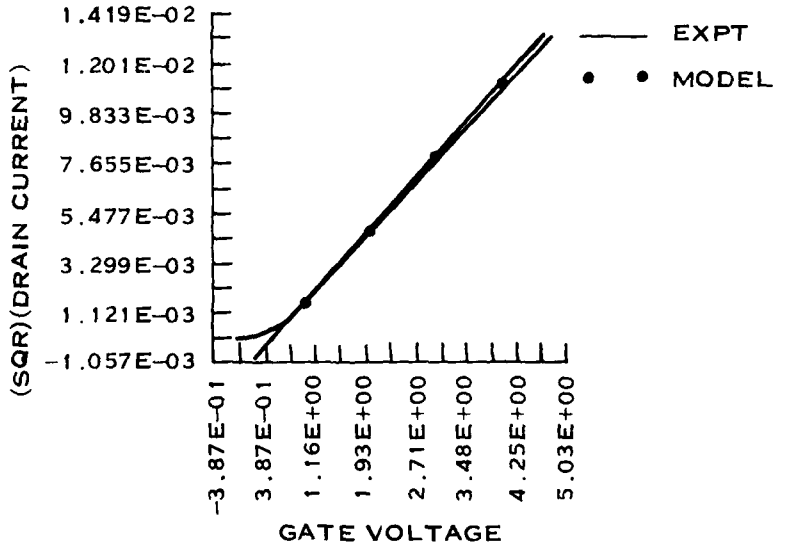


(B) EXPERIMENTAL CHARACTERISTICS WITH MODEL PREDICTIONS SUPERPOSED BY CIRCLES, SHOWING GOOD AGREEMENT (<15%)

Figure 19. Predicted I-V Characteristics of Device With Grounded Bulk



(A) I_D VS V_G CHARACTERISTICS IN THE LINEAR REGION ($V_S = V_B = V_X = 0V$, $V_D = 50$ MV)



(B) $\sqrt{I_D}$ VS V_G CHARACTERISTICS IN THE SATURATION REGION ($V_S = V_B = V_X = 0V$, $V_D = 5V$). THE MODEL PREDICTIONS AGAIN SHOW A FAVORABLE AGREEMENT

Figure 20. Close Correspondence of Predicted Presaturation and Postsaturation Function

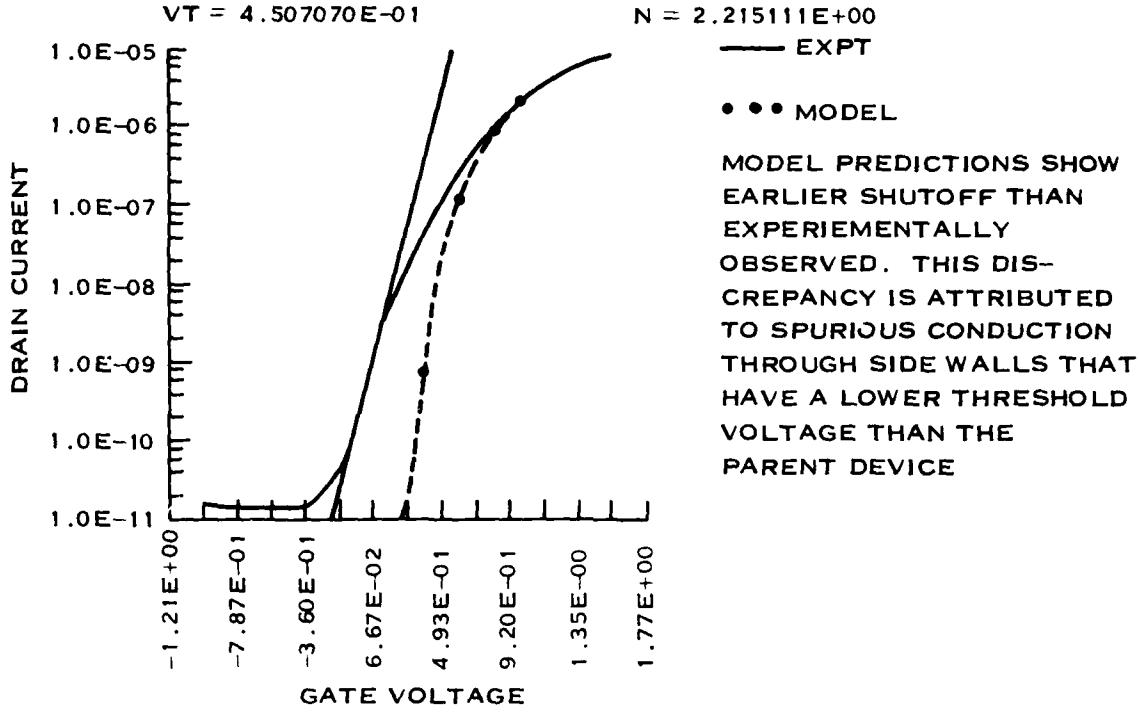


Figure 21. Experimental Weak Inversion Characteristics in Contrast to Model Predictions

An increase in negative bulk bias raises the channel depletion charge density through Equation (78), decreasing the available mobile charge density through Equation (69), resulting in less drain current. In other terms, with the negative applied bulk voltage, the back interface depletion collapses, allowing more depletion charge to be uncovered by the gate with the consequent reduction in mobile charge. With other device parameters held constant, a sudden decrease in the back interface fixed charge density by processing variations would result in a similar decrease in drain current. This points out the importance of achieving a tightly controlled back interface for reproducibility of device characteristics. The fixed charge density process variation generally tracks the absolute magnitude, and the achievement of low back interface fixed charge density is thought to be pivotal in SOI development.

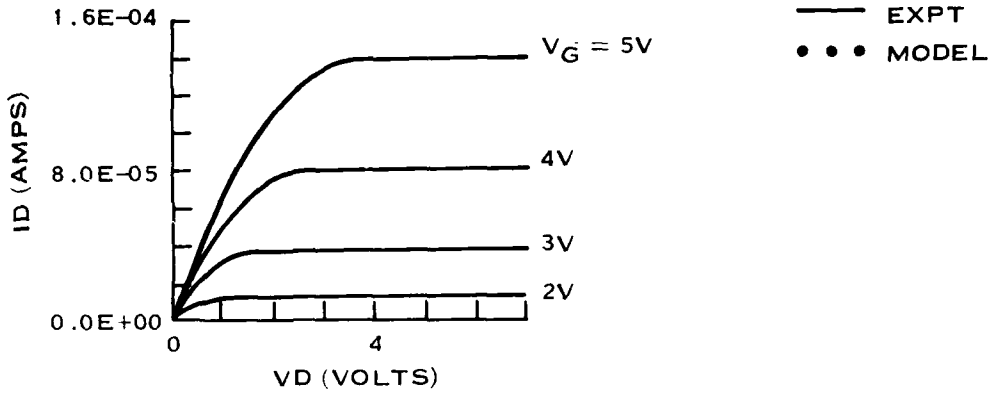
The present inavailability of SOI devices with a substrate terminal precludes the examination of the substrate bias effects. Table 1 summarizes some of the parameters.

2. Bulk Device Model Comparison

The verification of the model on bulk devices is presented in this subsection. Experimental data from n-channel devices fabricated in a bulk CMOS process with n^+ polygate self-aligned technology and LOCOS isolation was used.[29] The device parameters as extracted from the fabrication schedule, the test structures, and model comparison are listed in Table 2.

The actual impurity profile in the substrate is shown in Figure 23(a). The implanted profile near the surface was obtained from SUPREM simulation while the doping density deep in the substrate was

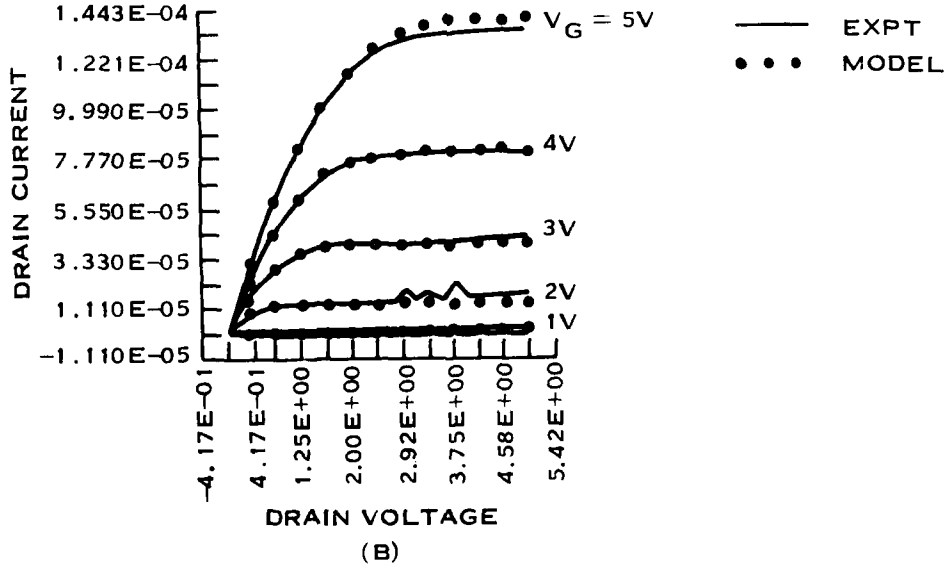
[29]D.B. Scott et al., IEDM Technical Digest (1981).



(A)

(A) THE MODELLED I-V CHARACTERISTICS OF SOI-MOSFET FOR V_B = -40V (V_S = V_X = 0V)

(B) THE EXPERIMENTAL I-V CHARACTERISTICS WITH SUPERPOSED PREDICTED DATA. COMPARING THIS WITH FIGURE 19 SHOWS THAT NEGATIVE APPLIED BULK VOLTAGE DECREASES DRAIN CURRENT. THIS IS AN ARTIFACT OF A DEVICE FEATURING SPACE-CHARGE INTERACTION BETWEEN GATE AND BULK TERMINALS.



(B)

Figure 22. Predicted Characteristics of Device With V_B = 40V

TABLE 2. SUMMARY OF N-CHANNEL BULK DEVICE PARAMETERS

Parameter	Value
W	60 μm
L	60 μm
x_o	590 nm
t_1	0.15 μm
t_2	200 μm
N_{A1}	1.6×10^{16} cm^{-3}
N_{A2}	4.5×10^{15} cm^{-3}
Q_{f1}	1.3×10^{-9} C cm^{-2}
V_c	20 V
μ_0	750 cm^2 V^{-1} s^{-1}

extracted from the substrate voltage sensitivity of the device threshold voltage obtained from the presaturation characteristics ($V_X = 0$ to -5 V, $V_D = 50$ mV). The step profile reduction of this impurity distribution is also shown in the figure. This was obtained from the procedure outlined in Appendix A. The validity of this procedure is evidenced in Figure 23(b) where the surface electric field as a function of surface potential is plotted for the two distributions, and a close fit is realized.

The gate oxide thickness was obtained from the accumulation MOS capacitance. The values for μ_0 and V_c were determined from a good match of the experimental presaturation I_D versus V_G plot with model predictions ($V_X = 0$ V, $V_D = 50$ mV).

Equation (77) was used to predict the device response. The accuracy of the model predictions is illustrated in Figures 24 and 25. The model has faithfully predicted the device response over a wide range of terminal voltages from weak inversion to strong inversion and from presaturation to postsaturation.

3. Projected SOI MOSFET Design Improvements

Having established the precision of the model in Subsections D.1 and D.2 above, this subsection is devoted to the investigation of the driving capability of an SOI device compared with a bulk device.

Three devices designed for identical threshold voltage are considered as shown in Figure 26:

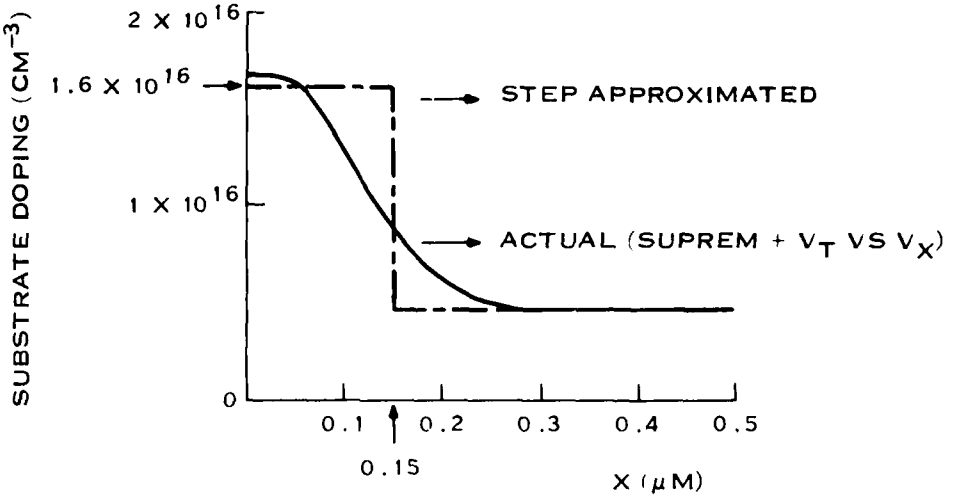
Device D1 is a bulk device.

Device D2 is an SOI device with a heavy back interface doping.

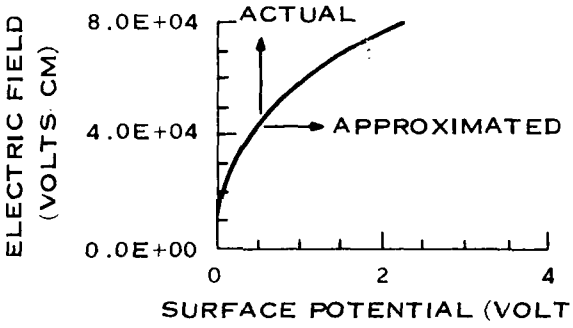
Device D3 is an SOI device that does not feature a heavy back interface doping.

The parameters of D1, D2, and D3 are summarized in Table 3. The predicted I-V characteristics of the devices are shown in Figure 27. Device D2 carries about 20 percent less drain current than D1 while D3 carries about 40 percent larger current ($V_G = V_D = 5$ V, $V_B = V_S = 0$ V). The reason for this outcome is revealed in Figure 28.

In Figure 28, the surface potential, the channel mobility, the normal and lateral electric fields, the depletion, and the mobile charge densities are plotted as a function of lateral position in the channel. All devices have the same surface potential at source, ϕ_{SS}; however, they differ in the surface potential at drain, ϕ_{SD}. This is the outcome of the charge neutrality relationship in Equation (69). Owing to small total dopant concentration in D3, it has the smallest Q_D. Because Q_m vanishes when the channel pinches off at drain, a smaller Q_D demands larger ϕ_{SD} through Equation (69). As a result, D3 has the highest lateral electric field, E_t. It also features the highest μ and Q_m. The drain current is a product of μ, Q_m, and E_t and



(A) ACTUAL SUBSTRATE IMPURITY PROFILE IN BULK-MOSFET AND ITS STEP APPROXIMATION USING PROCEDURE OF APPENDIX A.



(B) SURFACE ELECTRIC FIELD AS A FUNCTION OF SURFACE POTENTIAL FOR THE TWO PROFILES IS ALMOST IDENTICAL, A REQUIREMENT FOR FAITHFUL APPROXIMATION

Figure 23. Comparison of Effect of Negative Bias on Bulk to Reduce Drain Current

D3 naturally carries the largest current of the three devices discussed. The contrary remarks apply to D2, and it carries the lowest current.

The above analysis has assumed the same low field mobility for the three devices. A design such as D3 is possible only when the back interface fixed charge density is sufficiently low to not require a back channel suppressor implant. Under these conditions, D3 offers large improvement over D2 (70 percent larger I_D) and a significantly better driving capability than the bulk device D1 (40 percent larger I_D).

The channel mobility is a function of position in the channel, a feature of all devices, which has not been ignored in the mobility formulation of Equation (67). It is the exact calculation of the surface potentials ϕ_{SS} and ϕ_{SD} that has permitted the important differences in the three devices to be distinguished and the features of D3 to be decorated.

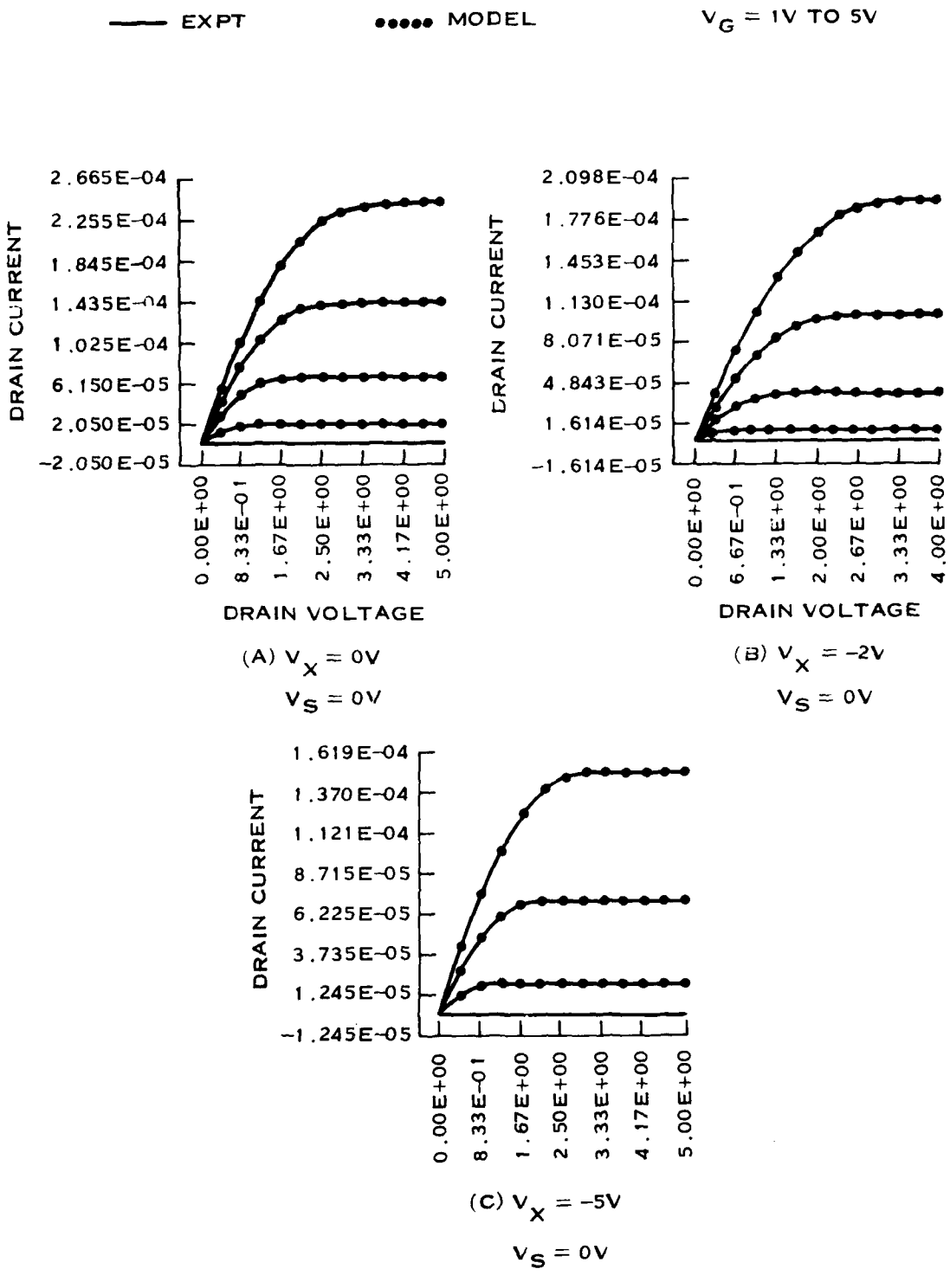


Figure 24. Model Comparison With Above-Threshold I-V Characteristics of Bulk MOSFET Under Various Substrate Biases

FIGURE 22 & 23 SHOW THAT THE MODEL FAITHFULLY PREDICTS DEVICE BEHAVIOR UNDER A WIDE VARIATION OF TERMINAL VOLTAGES.

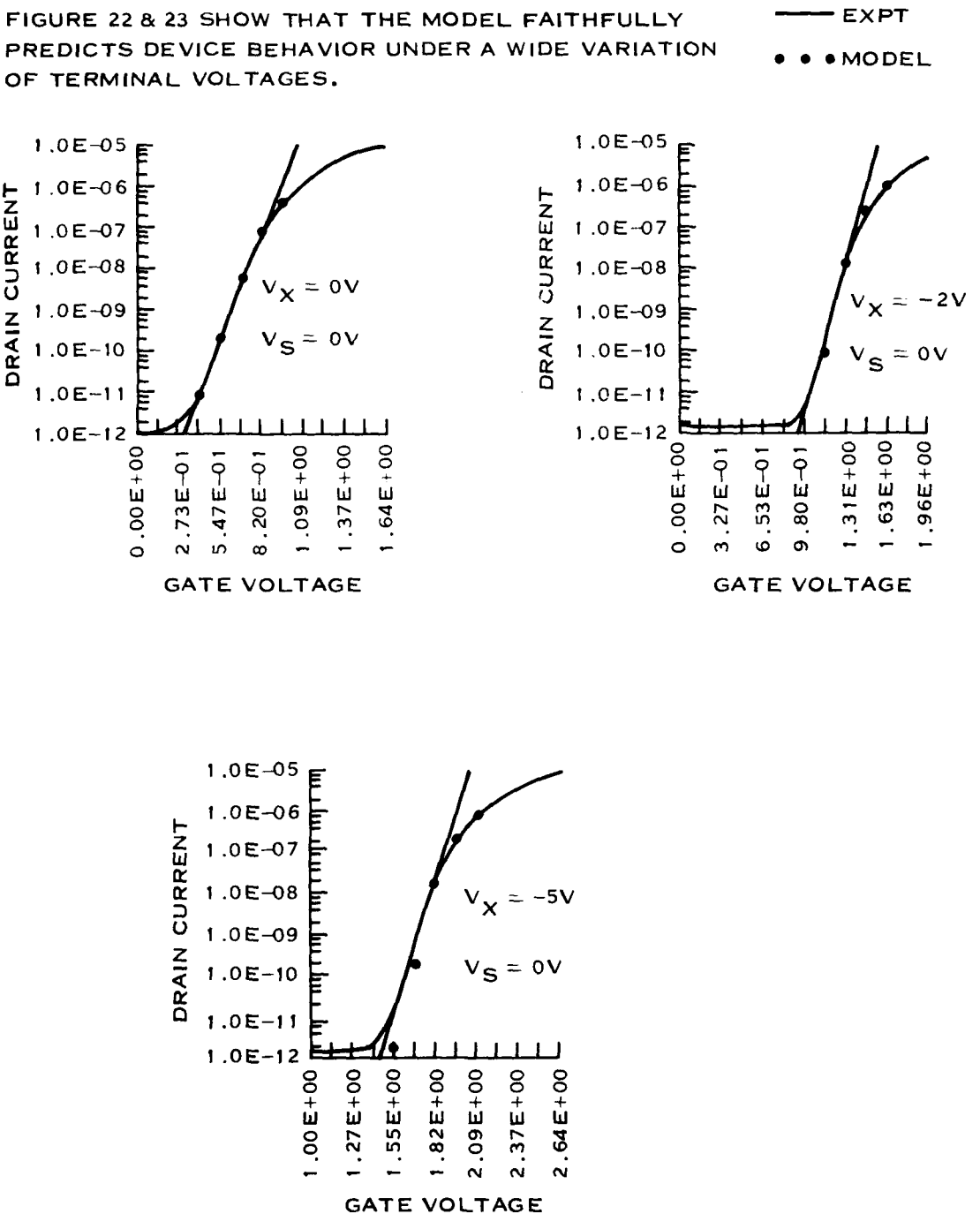
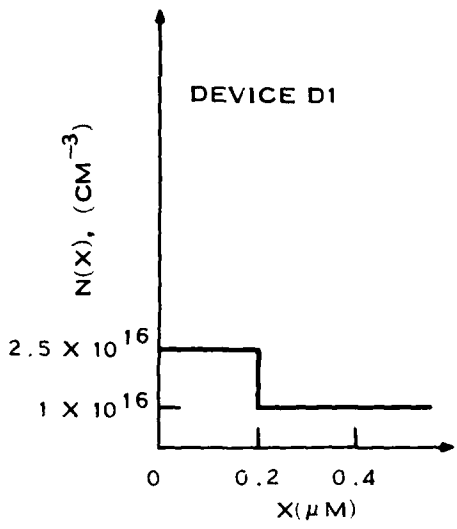
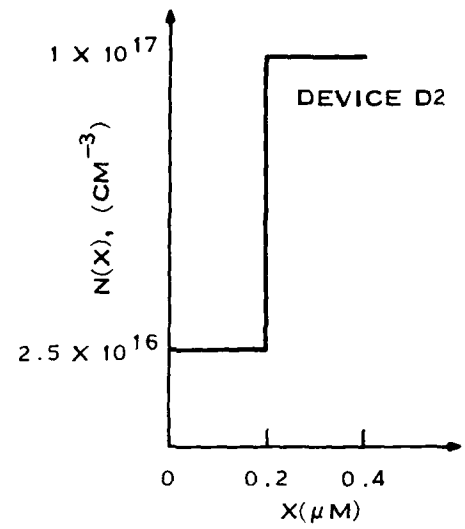


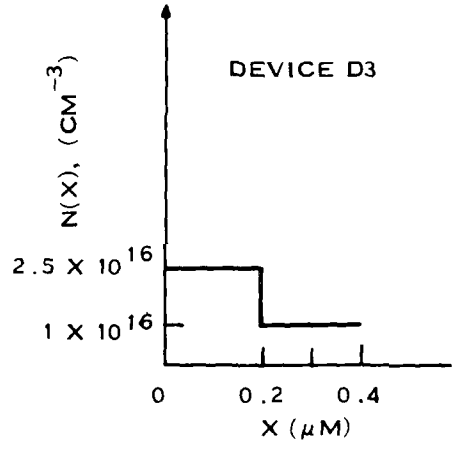
Figure 25. Model Comparison With Subthreshold Characteristics of Bulk MOSFET Under Different Substrate Biases



(A) BULK MOSFET D1



(B) SOI MOSFET WITH A HEAVY BACK CHANNEL SUPPRESSOR DOPING



(C) SOI MOSFET WITHOUT HEAVY DOPING AT BACK INTERFACE

Figure 26. Step Functions of Three Devices Designed for Identical Threshold Voltage ($V_S = V_X = 0$ V)

E. CONCLUSIONS

The silicon-on-insulator inversion-mode MOSFET structure has been analyzed in detail. Based on this analysis, an accurate drain current model for a long and wide channel device has been constructed. The model simulates the following features:

The effect of charge sharing between the gate and the bulk terminals of the device

The exact calculation of the surface potentials on the source and drain ends of the channel

An accurate formulation of the normal field dependence of the channel mobility

An analytical reduction of the implanted substrate distribution to a step profile

The effect of finite doping in the bulk on the back interface depletion.

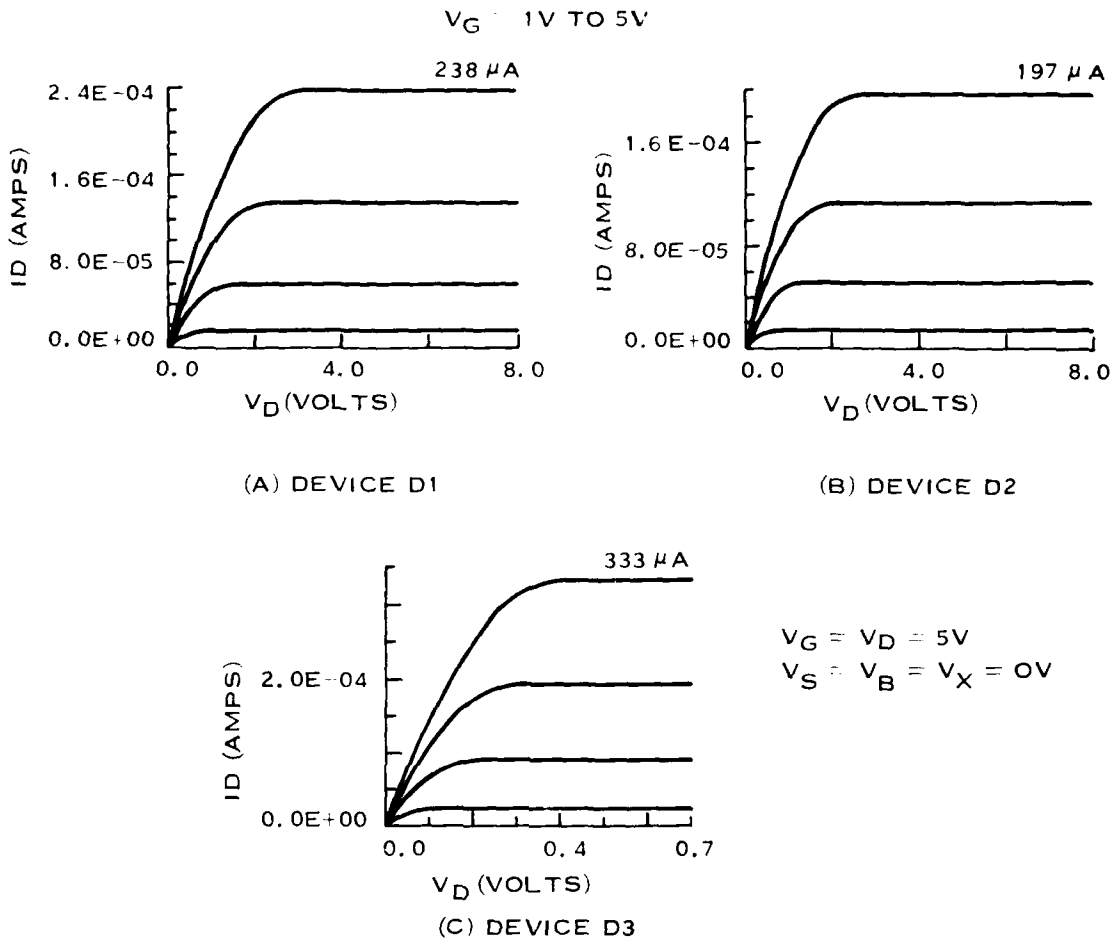
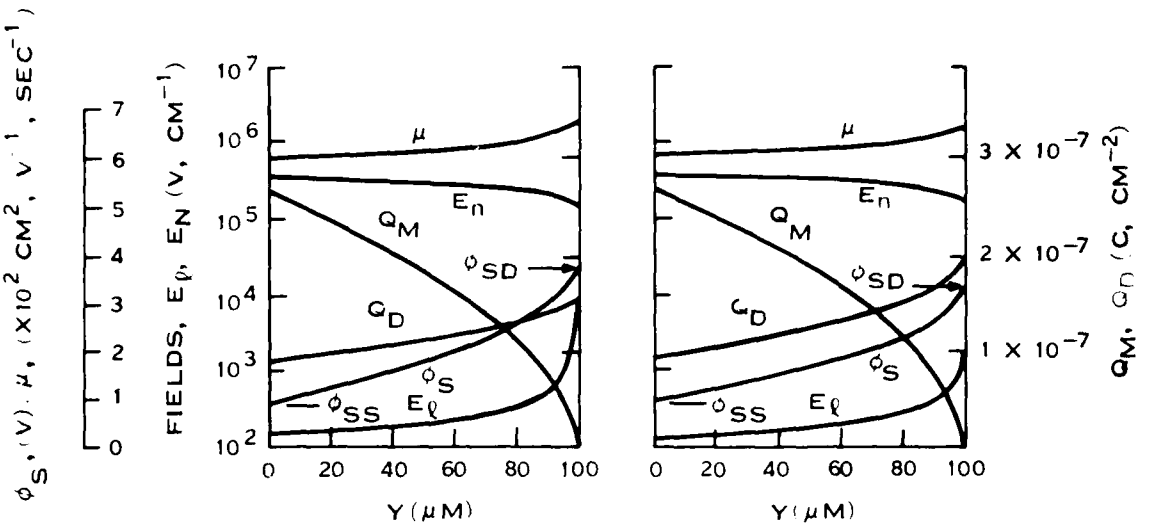


Figure 27. Modelled I-V Characteristics of Three Devices, Showing That D2 Carries About 20-Percent Less Drain Current Than D1 While D3 Carries About 40-Percent Larger Drain Current

Closed-form expressions for drain current are derived, in various regimes of device operation, that are valid from presaturation to postsaturation and from weak to strong inversion. Some of these expressions can also be used to model a bulk MOSFET.

The model has been verified against the available experimental data obtained from SOI and bulk devices.

Based on the information from this model and the experimental data, the following conclusions are drawn about the SOI MOSFET:



DEVICE D1

$V_G = 5V$

$V_S = V_B = V_X = 0V$

$I_D = 238\ \mu A$

(A)

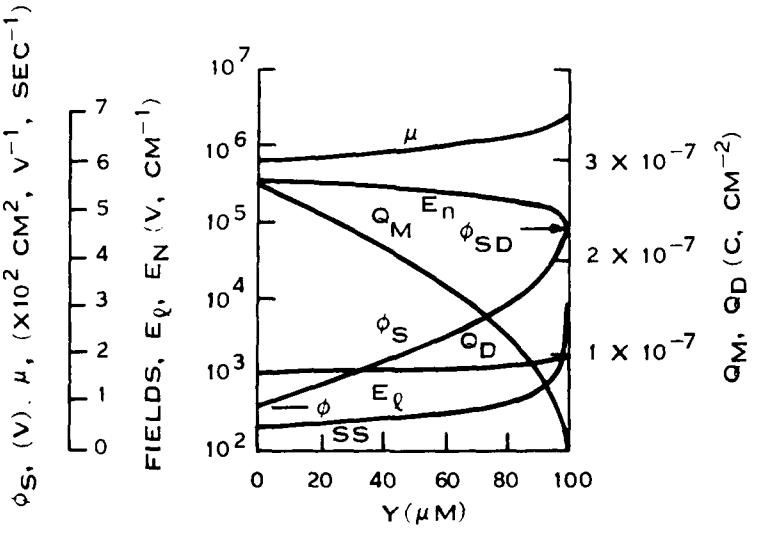
DEVICE D2

$V_G = 5V$

$V_S = V_B = V_X = 0V$

$I_D = 197\ \mu A$

(B)



DEVICE D3

$V_G = 5V$

$V_S = V_B = V_X = 0V$

$I_D = 333\ \mu A$

(C)

Figure 28. Parameters Versus Lateral Position in Channel for Same Surface Potential at Source

TABLE 3. SUMMARY OF DEVICE PARAMETERS ASSUMED FOR D1, D2, AND D3

Parameter	Value D1	D2	D3	Unit
W	100	100	100	μm
L	100	100	100	μm
C_{ox}	6.94×10^{-8}	6.94×10^{-8}	6.94×10^{-8}	F cm^{-2}
Q_{f1}/q	5×10^{10}	5×10^{10}	5×10^{10}	cm^{-2}
Q_{f2}/q	–	6.25×10^{11}	1×10^{11}	cm^{-2}
μ_n	750	750	750	cm^2 V^{-1} s^{-1}
V_t	20	20	20	V
N_{A1}	2.5×10^{16}	2.5×10^{16}	2.5×10^{16}	cm^{-3}
N_{A2}	1×10^{16}	1×10^{17}	1×10^{16}	cm^{-3}
t_1	0.2	0.2	0.2	μm
t_2	–	0.2	0.1	μm
t_{ox}	–	1.0	1.0	μm

The space charge interaction between the gate and the bulk terminals, if it occurs before device turnon, reduces the device threshold voltage and makes it more sensitive to parametric variations. An easy remedy to circumvent this enhancement sensitivity is to undertake a device design that precludes such interaction until after the device turnon.

The space charge interaction between the gate and the bulk terminals and the substrate exhaustion effects diminish the rate of increase of depletion charge associated to the gate terminal with increasing surface potential. This can give rise to a breakpoint in the square root of I_D versus V_G characteristics in saturation, increasing the slope. Such a device carries more current than a bulk device with the same substrate doping.

For a device featuring space charge interaction, a negative bulk voltage reduces the drain current of the device. This is a result of a collapse in the depletion layer created at the back interface by its fixed oxide charge density, causing the space charge interaction and the determinant bonus drain current to disappear.

Because of the reasons explained above, the device characteristics are sensitive to variations in the back interface fixed oxide charge density, tantamount to a change in the bulk voltage.

A heavy dose of back-channel suppressor implant reduces the drain current of the device. This is caused by the resulting reduced mobile channel charge density, channel mobility, and the lateral electric field in the channel. For a typical case studied, such a device carried 70 percent less drain current than a device that did not use the back-channel suppressor implant.

An SOI MOSFET that does not use a back-channel suppressor implant may take significant advantage of the space charge interaction and the substrate exhaustion effects to augment its drain current. For a typical case studied, the SOI MOSFET carried 40 percent more drain current than an equivalent bulk MOSFET at the same threshold voltage and channel mobility.

SECTION IV

BURIED CHANNEL MOSFET MODEL

A. INTRODUCTION

As a starting point for the development of a charge-sharing buried-channel model, a long-channel computer program has been written for the HP 1000 (Appendix G). This model has been extracted from the literature[30-33] and has the following features.

The actual implanted profile is approximated by a box distribution as shown in Figure 29. This approach cannot predict the threshold for surface p-type inversion in n-channel buried MOSFETs if the actual surface concentration is very different from the box concentration at the surface.

The computer program compares the gate voltage necessary to invert the surface, and thus lose control of the buried channel, with the gate voltage necessary to pinch off the device at the source. If the channel pinches off before the surface inverts, the current is assumed to be zero because there is presently no subthreshold model. If the surface inverts first, the current becomes independent of gate voltages less than the inversion voltage. Saturation is assumed to occur when the depletion layers from the substrate and from the surface just touch at the drain. The channel length modulation for the buried-channel model has not yet been included.

B. SURFACE CONDITION FOR DEVICE OPERATION

The linear region model predicts the current for the following surface conditions.

1. Inversion Along the Entire Surface

This inversion occurs in an n-channel device when the gate voltage is sufficiently negative that the surface potential equals that of the p-substrate. Under these conditions, holes will flow from the p-substrate through the channel stop region to the surface, thus clamping the surface potential to that of the substrate. Any further changes in gate voltage will have no effect on the n-channel region, so the drain current becomes independent of V_{GS}. The depletion layer between the surface and the channel will contain charge equal to

$$Q_Y = \sqrt{2\epsilon q N_D (V_Y + V_{BS} + V_{bi})} \tag{88}$$

where V_Y is the voltage of the channel. The charge on the gate at the inversion condition is

$$Q_G = C_o (V_{GS} + V_{BS} - V_{fb} + V_{bi}) \tag{89}$$

[30]J.S.T. Juang and G.W. Taylor, "Modeling of an Ion-Implanted Silicon-Gate Depletion-Mode IGFET," *IEEE Trans. Electron Devices* **ED-22** (1975) pg 995.

[31]J.R. Edwards and G. Marr, "Depletion-Mode IGFET Mode by Deep Ion-Implantation," *IEEE Trans. Electron Devices* **ED-20** (1973) pg. 283.

[32]Y.A. El-Mansy, "Analysis and Characterization of the Depletion-Mode IGFET," *IEEE J. Solid State Circuits* **15** (1980) pg 331.

[33]G. Merckel, "Ion Implanted MOS Transistors—Depletion Mode Devices," Proceedings of NATO Advanced Study Institute, Process and Device Modeling for Integrated Circuit Design, Editors Fernand Van De Wele et al., July 19–29, 1977, Louvain-la-Neuve, Belgium.

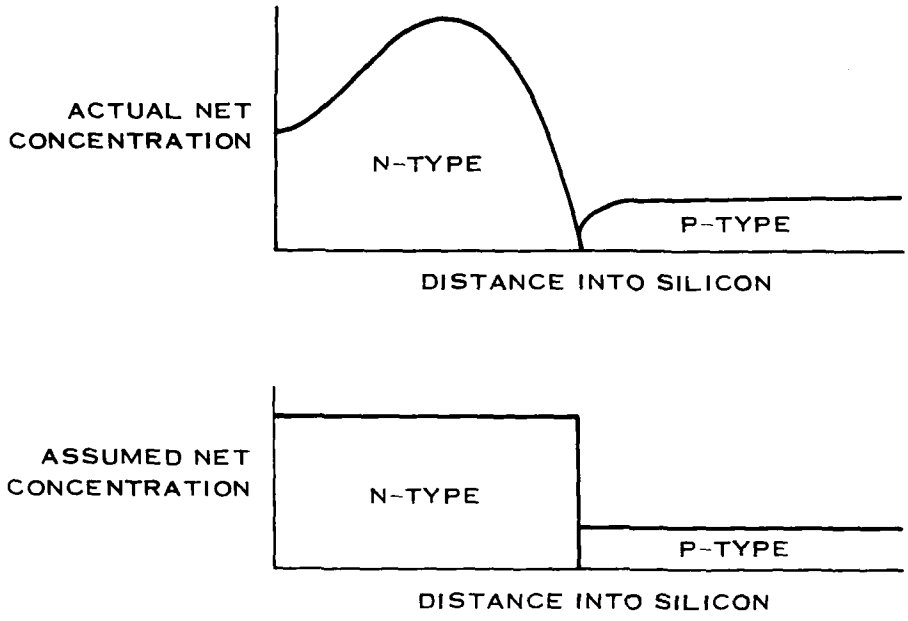


Figure 29. Actual and Assumed Distributors of Impurities in Silicon

where V_{fb} is the flat band voltage and V_{bi} is the built-in voltage between the n-channel and the p-substrate. If inversion occurs at the drain, the entire surface will be inverted; thus,

$$C_o(V_{GS} + V_{BS} - V_{fb} + V_{bi}) \leq \sqrt{2\epsilon q N_D(V_{DS} + V_{BS} + V_{bi})} \tag{90}$$

and the threshold for inversion at the drain can be defined as

$$V_{TID} = \frac{\sqrt{2\epsilon q N_D(V_{DS} + V_{BS} + V_{bi})}}{C_o} - V_{BS} + V_{fb} - V_{bi} \tag{91}$$

resulting in a definition of this region as

$$V_{GS} \leq V_{TID} \tag{92}$$

2. Inversion at the Source With Depletion at the Drain

This inversion occurs when the voltage drops along the channel. If $V_{DS} = 0$, the entire surface will be inverted. However, the depletion layer thickness at the drain between the channel and the surface increases as V_{DS} satisfies Equation (91); all the inversion charge at the drain will be replaced with depletion charge, and the surface potential will no longer be clamped to the substrate potential. Any further increases in V_{DS} will cause the edge of the inversion layer to move from the drain toward the source. A threshold for inversion at the source can be defined as

$$V_{TIS} = \frac{\sqrt{2\epsilon q N_o(V_{BS} + V_{bi})}}{C_o} - V_{BS} + V_{fb} - V_{bi} \tag{93}$$

and thus the definition of this region becomes

$$V_{TID} < V_{GS} \leq V_{TIS} \tag{94}$$

3. Depletion Along the Entire Surface

Depletion along the entire surface occurs when V_{GS} is high enough to not invert the source end of the surface but is low enough that accumulation does not begin to occur at the source. Accumulation will begin to occur at the source when $V_{GS} \geq V_{fb}$. This region is defined by

$$V_{TIS} < V_{GS} \leq V_{FB} \tag{95}$$

4. Accumulation at the Source and Depletion at the Drain

Accumulation at the source and depletion at the drain occur when V_{GS} is high enough to cause accumulation at the source but V_{DS} is large enough that no accumulation occurs at the drain; thus,

$$V_{FB} < V_{GS} \leq V_{DS} + V_{FB} \tag{96}$$

5. Accumulation Along the Entire Surface

Accumulation along the entire surface will be assured if the drain end is accumulated. This occurs for

$$V_{DS} + V_{FB} < V_{GS} \tag{97}$$

The derivation of the current equations is the same as that for enhancement devices except accounting for the surface charge.

$$I_D = \mu_B \frac{W}{L} \left\{ qN_D X_j V_{DS} - \frac{2}{3} \sqrt{2\epsilon q \left(\frac{N_A N_D}{N_A + N_D} \right)} \left[(V_{DS} + V_{BS} + B_{bi})^{3/2} - (V_{BS} + V_{bi})^{3/2} \right] - Q_{YSD} - \frac{\mu_S}{\mu_B} Q_{YSA} \right\} \tag{98}$$

where μ_B and μ_S are the bulk and surface mobilities and

$$Q_{YSD} = \int Q_D \, dV \text{ and } Q_{YSA} = \int Q_A \, dV \tag{99}$$

where Q_d is the surface depletion charge and Q_A is the surface accumulation charge.

C. SHORT CHANNEL EFFECTS IN DEPLETION DEVICES

1. Double Charge-Sharing Effect

Understanding the short-channel effects in these devices is necessary to accurately model small geometry circuits. The turnon characteristics of these devices at 0.5- to 4-μm channel length have been extensively studied to develop the two-dimensional charge-sharing mechanism in buried-channel transistors. The dependence of V_T on gate length for both buried-channel MOSFETs and MESFET devices is

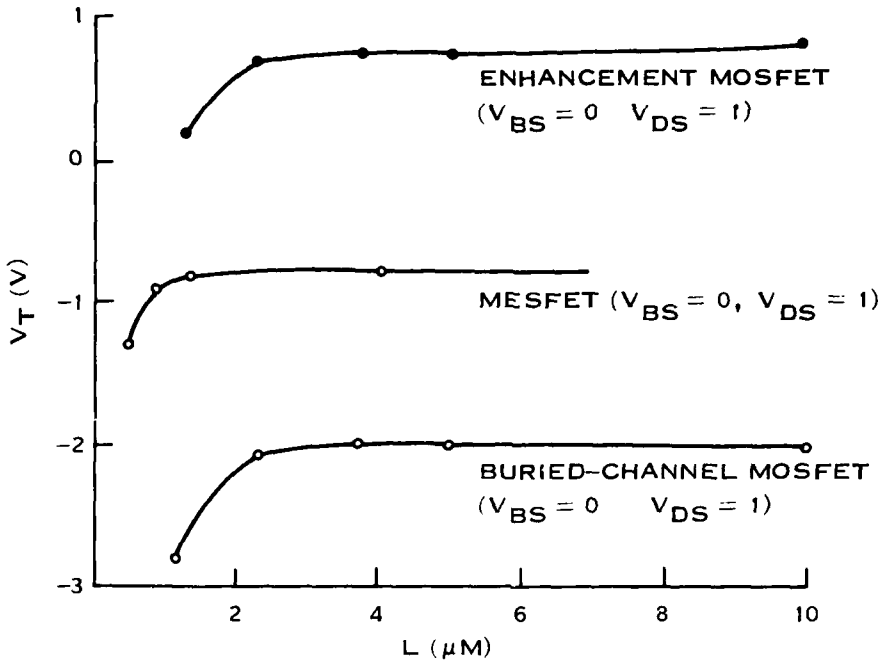


Figure 30. Threshold Dependence on Channel Length—Comparision of Enhancement and Buried-Channel MOSFETs and MESFETs

shown in Figure 30. For comparison, Figure 30 also includes the channel length dependence of V_T of an enhancement MOSFET of similar doping levels. The similarity of the behavior of the buried-channel structure and the enhancement devices shows that the charge-sharing principles used to model the two-dimensional effects in a short-channel enhancement device are also applicable to the buried-channel device. However, the MESFET does show a significantly smaller short-channel V_T reduction.

Figure 31 compares the body effect b as a function of gate length for buried-channel MOSFETs and MESFET structures. We define body effect as

$$b = \frac{dV_t}{d\sqrt{V_{BS} + V_{bi}}} \tag{100}$$

Note that the body effect increases at small channel length for MESFETs whereas it decreases for MOSFETs. A formulation for the buried channel charge-sharing mechanism has been established on the basis of these data.

The short-channel formulation for the buried-channel structure may be developed based on an extension of the two-dimensional charge-sharing theory. The length dependence of the body effect for the MESFET and buried-channel MOSFET suggests that there are two charge-sharing mechanisms.

Figure 32(a) shows the trapezoidal charge sharing for the enhancement MOSFET. The gate-controlled charge is represented by the trapezoid. Figure 32(b) shows the MESFET cross section. The n^+ source and drain regions are separated from the gate edge in the MESFET because self-aligned Schottky barrier gates cannot be easily fabricated. The gate thus controls the additional depletion charge at the channel edges, and the back junction determines the edge of the bottom depletion region where the

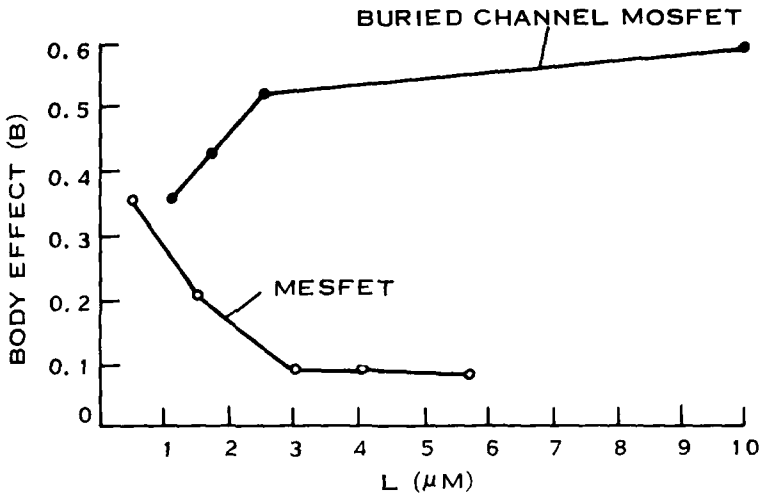


Figure 31. Channel Dependence of Body Effect for Buried-Channel MOSFETs and MESFETs

normal enhancement type of charge sharing takes place. If $L' \simeq L$, then the enhancement charge-sharing factor for the effective gate length L of a MESFET is on the order of the similar factor for an enhancement MOSFET of length $3L$. In addition, the gate controls the extra amount of depletion charge caused by the fringing effect. Thus, MESFETs of comparable gate length show less short-channel effects than enhancement MOSFETs.

For the self-aligned gate buried-channel MOSFET [Figure 32(c)], the enhancement charge-sharing factor is the same as for the enhancement MOSFET, but the depletion fringing provides some extra charge so that the net short-channel effect in buried-channel devices is slightly smaller than in enhancement devices.

This formulation also explains the anomalous body effect data for MESFETs. The substrate bias primarily affects the enhancement charge-sharing factor; therefore, it reduces the body effect for buried channel MOSFETs whereas it adds to the fringing charge in a MESFET and does not significantly change the enhancement charge-sharing of the nonself-aligned feature.

We may formulate the threshold of the buried-channel structure as follows. The depletion edge X'_n may be determined by the trapezoidal charge-sharing factor F_E as in the enhancement case. Referring to Figure 32(c),

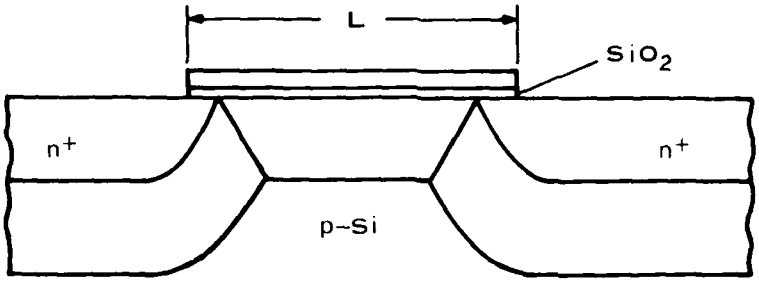
$$d' = d - X_n = d - \frac{N_A}{N_D}\sqrt{K_A(V_{BS} + V_{bi})}\,F_E \tag{101}$$

The charge balance at $V_G = V_T$ for $V_{DS} \gg 0$ may be written as

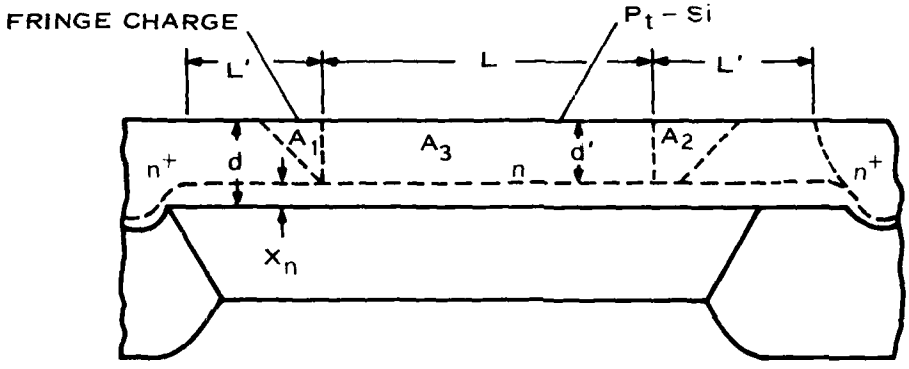
$$\sqrt{\frac{2\epsilon}{qN_D}(V_T - V_{bi})}\,qN_D L = \frac{qN_D d'}{2}\left\{2L + d' + \sqrt{K_D V_{DS}} + \sqrt{d'^2 + K_D V_{DS}}\right\} \tag{102}$$

where

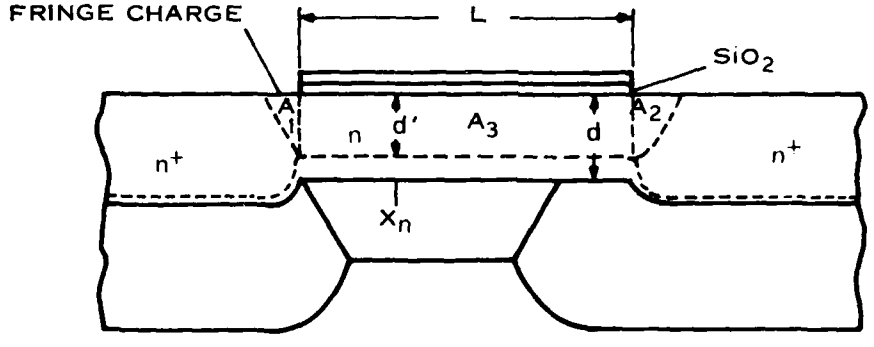
$$K_{A(D)} = \frac{2\epsilon}{qN_{A(D)}}$$



(A) ENHANCEMENT MOSFET



(B) MESFET



(C) BURIED CHANNEL (DEPLETION) MOSFET DEVICES

Figure 32. Two-Dimensional Charge-Sharing in Enhance and Buried-Channel MOSFETs and MESFETs

Thus,

$$V_t = V_{bi} - \frac{qN_D}{2\epsilon}(d' F_D)^2 \tag{103}$$

where

$$F_D = \left[1 + \frac{d'}{2L} + \frac{1}{2L}\sqrt{K_D V_{DS}} + \frac{1}{2L}\sqrt{d'^2 + K_D V_{DS}^2}\right] \tag{104}$$

Substituting Equation (101) in Equations (103) and (104), we may write the expression for the short-channel V_t of a buried-channel device as

$$V_t = V_{bi} - \frac{d^2}{K_D} F_D^2 + \frac{2}{K_D} \cdot \frac{N_A}{N_D}\sqrt{K_A(V_{BS} + V_{bi})}\, F_E F_D^2 \tag{105}$$

where

$$F_D = \left[1 + \frac{1}{2L}\left(d - \frac{N_A}{N_D}\right)\sqrt{K_A(V_{BS} + V_{bi})}\, F_E + \sqrt{K_D V_{DS}}\right.$$

$$\left. + \sqrt{d^2 - \frac{2dN_A}{N_D}\sqrt{K_A(V_{BS} + V_{bi}) + K_D V_{DS} + \left(\frac{N_A}{N_D}\right)^2 K_A(V_{BS} + V_{bi})}}\right] \tag{106}$$

and F_E is the trapezoidal enhancement charge-sharing factor.

D. NONEQUILIBRIUM PHENOMENA

The subthreshold and near-threshold characteristics of buried-channel MOSFETs have shown some interesting nonequilibrium characteristics, which are attributable to the injection and trapping of holes at the Si/SiO_2 interface from the channel stop regions. Effects of the deep depletion of the surface p-channel have been studied, and the I-V characteristics shown in Figure 33 indicate that such effects result in anomalous turnoff characteristics that are strongly dependent on history of the gate voltage and drain voltage excursions. Such phenomena make it difficult to measure the normal subthreshold characteristics of buried-channel devices and will interfere in circuit operation, especially for load devices. A systematic study of the physics of the channel modulation of this hole current is necessary to design buried-channel device structures or circuits that circumvent these problems.

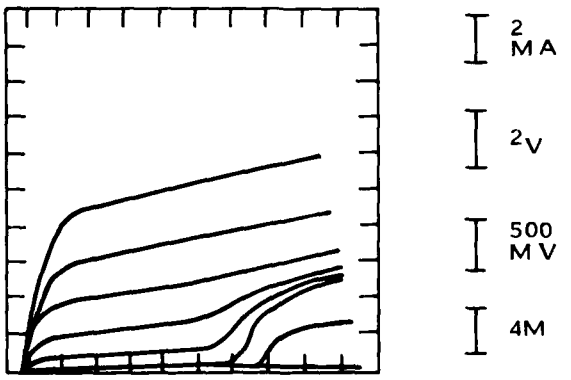


Figure 33. Anomalous I-V Characteristics of Buried-Channel MOSFETs Near Turnoff, Showing Nonequilibrium Effects

SECTION V

SCALABILITY OF N-CHANNEL AND P-CHANNEL MOSFETS

A. INTRODUCTION

MOS device scaling for higher density and improved performance has been a goal of present technology for VLSI. With the development of high-resolution lithography systems, it has been possible to fabricate devices with micrometer and submicrometer geometries. The original concepts for scaled MOS devices as presented in 1974[34] are based on scaling down the horizontal and vertical dimensions, together with the voltage applied to the device, by the same scaling factor. This scaling would lead to higher device gain, shorter circuit delay time, and reduced power dissipation. However, to maintain TTL compatibility and considering noise margin, there has been a general reluctance to scale down the operating voltage by original scaling law. Nonscalability of voltages, however, results in higher electric fields inside the MOSFET device, which degrades its performance.[35,36] Another problem of device scaling is the increasing importance of parasitic effects, such as contact resistance, source/drain diffusion resistance, and inversion layer capacitance.[36] Because these quantities do not scale proportionately with physical dimensions, the device performance might eventually be dominated by these parasitic effects.

Although there has been considerable effort[35,36] to clarify the scalability limit of MOS devices, there are several reasons why the issue needs to be reexamined at this time.

- New data on the velocity-field characteristics of surface electrons and holes in silicon is available.[37]
- The limitation on the series resistance of source/drain ion-implanted junctions is much more severe[38,39] than had been previously assumed.[35,36]
- A new transmission line model has been developed to analyze the series resistance of the source/drain region with silicide.[40]

In this analysis, these factors have been taken into account and the device performance of both n-channel and p-channel MOS devices has been reconsidered along the lines of the three scaling laws discussed by Chatterjee, et al.[35] In Subsection B these scaling laws are explained. Next, Subsection C describes an optimal device structure for scaled MOS devices. In Subsection D the various parasitic effects that affect the device performance are explained, including the series resistance of ion-implanted junctions, the contact resistance between metalization and ion-implanted junctions and/or between silicide and ion-implanted junctions, mobility rolloff caused by both lateral and transverse electric fields, and finite inversion layer thickness.[36] Then, in Subsection E, the device performance is considered in relation to these factors. The relative importance of each factor, as a function of the scaling factor is discussed. Conclusions suggesting the relative importance of technology enhancements to address these

[34]R.H. Dennard, F.H. Gaensslen, H.N. Yu, V. Rideout, E. Bassous, and A.R. LeBlanc, "Design of Ion-Implanted MOSFETs With Very Small Physical Dimensions," *IEEE J. Solid-State Circuits* SC-9 (October 1974) pp. 256–268.

[35]P.K. Chatterjee, W.R. Hunter, T.C. Holloway, and Y.T. Lin, "The Impact of Scaling Laws on the Choice of N-Channel or P-Channel for MOS VLSI," *IEEE Electron Device Lett.* ELD-1 (October 1980) pp. 220–223.

[36]Y.A. El-Mansy, "On Scaling MOS Devices for VLSI," *Proceedings of ICCC Conference*, Poughkeepsie, NY (1980) pp. 457–460.

[37]R.W. Coen and R.S. Muller, "Velocity of Surface Carriers in Inversion Layers on Silicon," *Solid-State Electron.* 23 (1980) pp. 35–40.

[38]D.B. Scott, "An Examinzation of the Effect of P+ Source-Drain Limitations on P-Channel Scaling in CMOS," Texas Instruments Technical Report, TR-08-80-34 (January 1981).

[39]H. Schichijo unpublished data.

[40]D.B. Scott, W.R. Hunter, and H. Shichijo, "A New Transmission Line Model for Silicided Diffusions: Impact on the Performance of VLSI Circuits," *Dig. Tech. Papers* 1981 Symposium on VLSI Technology, Maui (September 1981).

limitations, are formulated to guide future research and development efforts. The analysis is phenomenological in that various assumptions have been adopted that best reflect the industrial trend of scaled MOS technology. Although these assumptions may not be rigidly adhered to as technology evolves, nonetheless, it is felt that the conclusions summarized in Subsection F will have general validity.

B. DEVICE SCALING

1. Classical Scaling

The principle of classical MOS device scaling[34] is to reduce all horizontal dimensions, vertical junction depths and gate oxide thickness, and the voltages by a common scaling factor κ ($\kappa < 1$) while increasing the doping proportionately so that the electric field inside the device is unchanged. This can be seen from the relations:

$$E = \frac{\partial \psi}{\partial x} \tag{107}$$

and

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{q}{\epsilon_{Si}} N_A \tag{108}$$

where E and ψ are the electric field and potential, respectively, and N_A is the doping concentration. A one-dimensional form is used to facilitate the notation. From Equation (107), when the linear dimension is scaled down, i.e., $x' = \kappa x$ (the primed quantities refer to the new scaled device parameters), the voltage must be scaled down by the same factor, i.e., $\psi' = \kappa\psi$, to keep the electric field unchanged. To accomplish this, as seen from Equation (108) the doping, N_A, must be increased by the same factor, i.e., $N'_A = N_A/\kappa$. Keeping the electric field distribution unchanged avoids unnecessary and undesirable high-field effects, such as mobility degradation from velocity saturation, impact ionization, and hot electron injection into the gate oxide.

One important consequence of this classical scaling, commonly referred to as "constant field scaling," is that the depletion layer widths in the scaled-down device also approximately scale proportionately with the other horizontal dimensions as seen for the case of the drain-substrate depletion layer

$$\begin{aligned} W'_d &= \left[\frac{2\epsilon_{Si}}{qN_A}(V_{bi} + V'_{BS} + V'_{DS})\right]^{1/2} \\ &= \left[\frac{2\epsilon_{Si}\kappa}{qN_A}(V_{bi} + V_{BS} + V'_{DS})\right]^{1/2} \sim \kappa W_d \end{aligned} \tag{109}$$

where W_d is the depletion layer width, V_{bi} is the junction built-in potential, V_{DS} is the drain-source voltage, and V_{BS} is the substrate bias voltage. Without this scaling of the depletion widths, the depletion regions from the source and the drain merge together as the gate length is scaled-down and punchthrough results. Strictly speaking, however, this scalability of the depletion layer widths only holds for the case when the applied voltage is much larger than the built-in potential, i.e., $V'_{DS} >> V_{bi}$ and $V'_{BS} >> V_{bi}$, as seen in Equation (109). The built-in potential, V_{bi}, which is approximately given by

$$V_{bi} \sim \frac{2kT}{q} \ln \frac{N_A}{n_i} \tag{110}$$

does not scale down with other quantities. One consequence of this fact is that the doping concentration must be scaled by N_A/κ^n where $n > 1$ as shown later.*

Another quantity that fails to scale is the slope of the subthreshold transfer characteristics.[34] The inverse semilogarithmic slope, α, which is given by[41]

$$\alpha = \frac{dV_G}{d(\log_{10} I_{DS})} = \frac{2.3\,kT}{q}\left(1 + \frac{C_d + C_{is}}{C_{ox}}\right) \tag{111}$$

remains the same as for the unscaled device. Here C_{ox} is the gate oxide capacitance, and C_d and C_{is} are the capacitances of bulk depletion charge and fast surface states, respectively. The value of α determines the leakage current in the normally off device, which is an important parameter in considering refresh time in dynamic circuits or standby power dissipation in static circuits (especially CMOS circuits). For example, the standby power dissipation in CMOS circuits can be expressed as[38]

$$P_s = N\left(\frac{W}{L}\right) V_{DD}\, 10^{-} \exp\left(\frac{-V_T}{0.43\,\alpha}\right) \tag{112}$$

where N is the number of devices on a circuit, W and L are the width and channel length of the individual device, V_{DD} is the supply voltage, and V_T is the threshold voltage. As seen in Equation (112), the scaling of V_T with α being kept constant poses a serious problem. Therefore, the nonscalability of subthreshold characteristics limits the constant field scaling approach. *Conceptually*, a better scaling can be realized by lowering the operating temperature,[34] i.e., $T' = \kappa T$, as seen in Equations (110) and (111). There is experimental evidence[42] for the improvements in device characteristics at lower temperatures. Such an approach, however, is impractical at present and is not considered further.

2. Alternative Scaling

As shown in the previous section, a straightforward constant field scaling is not always desirable from a practical point of view. Additionally, in practice the choice of supply voltage is dictated by other overriding considerations, such as interface (TTL) compatibility and noise margins. Therefore, it is necessary to consider more realistic scaling scenarios that deviate from idealized constant field scaling. Recently, Chatterjee, et al.[35] has considered three different scaling schemes in which gate oxide thickness, channel doping, and supply voltage scale as different simple functions of a scaling factor, κ. It is not obvious, however, that such scalings, although simple, give optimal device parameters for scaled devices in terms of short-channel effects and threshold voltage. To this end, we consider more realistic, "externally forced" scaling scenarios with the following conditions.

a. Condition 1

The sum of source and drain depletion widths, $W'_d + W'_n$, scales down proportionately with other horizontal dimensions. W'_d is given by Equation (109) and W'_s is given by

$$W'_s = \left[\frac{2\epsilon_{Si}}{qN_A}(V_{bi} + V'_{BS})\right]^{1/2} \tag{113}$$

This condition assures that the scaled device still maintains long-channel behavior without punchthrough. It has been shown[43] that this one-dimensional estimate gives lower punchthrough voltages than the result from two-dimensional device simulation. In other words, this condition is too restrictive to prevent the punchthrough. This seems to agree with the empirical scaling relation,[44] which states that if

[41] R.M. Swanson and J.D. Meindl, "Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits," *IEEE J. Solid-State Circuits* **SC-7** (April 1972) pp. 146–153.

[42] F.H. Gaensslen, V.L. Rideout, E.J. Walker, and J.J. Walker, "Very Small MOSFETs for Low-Temperature Operation," *IEEE Trans. Electron Devices* **ED-24** (March 1977) pp. 218–229.

[43] J.J. Barnes, K. Shimohigashi, and R.W. Dutton, "Short-Channel MOSFETs in the Punchthrough Current Mode," *IEEE Trans. Electron Devices* **ED-26** (April 1979) pp. 446–453.

[44] J.R. Brews, W. Fichtner, E.H. Nicollian, and S.M. Sze, "Generalized Guide for MOSFET Miniaturization," *IEEE Electron Device Lett.* **EDL-1** (January 1980) pp. 2–4.

the junction depth and the gate oxide thickness are scaled linearly, the sum of depletion widths, $W'_d + W'_s$, needs only to scale as $\kappa^{2/3}$ instead of linearly. For analytical simplicity, however, condition 1 is used in this work with the understanding that the condition is slightly too restrictive.

b. Condition 2

The threshold voltage, V_t, scales with the supply voltage, V_{DD}, maintaining $V_t = 0.2\ V_{DD}$. The threshold voltage is given by

$$V_t = \phi_{ms} + \frac{Q_f}{C_{ox}} + 2\phi_f + \frac{1}{C_{ox}}\sqrt{2\epsilon_s qN_a(2\phi_f)} \tag{114}$$

where Q_f is the fixed oxide charge density and $\phi_f = (kT/q) \ln (N_a/n_i)$.

Given these two conditions and scaling schemes of the supply voltage, the gate oxide thickness and the doping are determined uniquely as a function of scaling factor. Here we adopt three scaling scenarios of power supply voltage described by Chatterjee, et al.:[5] a constant field scaling (CE) in which the voltage scales as κ, a constant voltage scaling (CV) in which the voltage is constant, and a quasi-constant voltage scaling (QCV) in which the voltage scales as $\kappa^{1/3}$. Unscaled ($\kappa = 1$) values of $V_{DD} = 5$ V and $V_t = 1$ V for a patterned gate length of 3 μm are assumed. The doping concentration for an unscaled device has been optimized using a two-dimensional numerical analysis[4] to give $I/W = 1 \times 10^{-9}$ A/μm with $V_{DS} = 5$ V, $V_{GS} = 0$ V, and $V_{BS} = 0$ V. The resulting doping concentration is $N_a = 4 \times 10^{15}$ cm^{-3} and, therefore, the one-dimensional estimate by Equations (109) and (113) gives $W_s + W_d = 1.83$ μm for an unscaled device.

Shown in Figures 34 and 35 are the doping and gate oxide thickness, respectively, calculated from these scaling schemes as a function of gate length, or scaling factor κ under zero substrate bias, i.e., $V_{BS} = 0$ V. Even for a constant field scaling, the doping needs to be scaled more rapidly than $1/\kappa$ because of nonscalability of the junction built-in potential.* The gate oxide thickness of 900 nm for 3-μm gate length appears to be too large when compared to the current technology, which uses 400 $\sim$ 600 nm of gate oxide. However, if one takes into account the lateral diffusion of source/drain dopants (80 percent of the junction depth), the actual channel length would be approximately 2 μm. For this channel length, Figure 35 gives a gate oxide thickness of 500 $\sim$ 600 nm, which is consistent with the thickness commonly used. In Subsection E, these parameters are used to examine the performance of a scaled device under the three scaling scenarios described above.

C. DEVICE STRUCTURE

As device dimensions are scaled down, some modifications to the device structure are necessary to take full advantage of the scaling. For example, a device structure for 5-μm gate length may not be the optimal structure for 0.5-μm gate length. This subsection describes some of the structure issues, and discusses an optimal device structure for submicrometer MOS devices. First, consider a classical unscaled device structure as shown in Figure 36(a), employing an n^+ implant self-aligned to the patterned polygate. There are several disadvantages in employing the same structure in scaled devices.

With a decrease of junction depth, as required to reduce short-channel effects, the increasing sheet resistivity of diffused junctions hamper their use as interconnect lines.

The large gate/drain overlap capacitance, while reduced by the self-aligned implant, is still finite and limits the switching speed of the device.

When the supply voltage is not scaled down, the high electric field at the drain end causes impact ionization and hot electron trapping.

The structure is not compatible with silicide technology. It is difficult to form silicide on the source/drain region without shorting them to gate polysilicon.

*J.A. Greenfield and R.W. Dutton, "Nonplanar VLSI Device Analysis Using the Solution of Poisson's Equation," *IEEE Trans. Electron Devices* **ED-27** (August 1980) pp. 1520–1532.

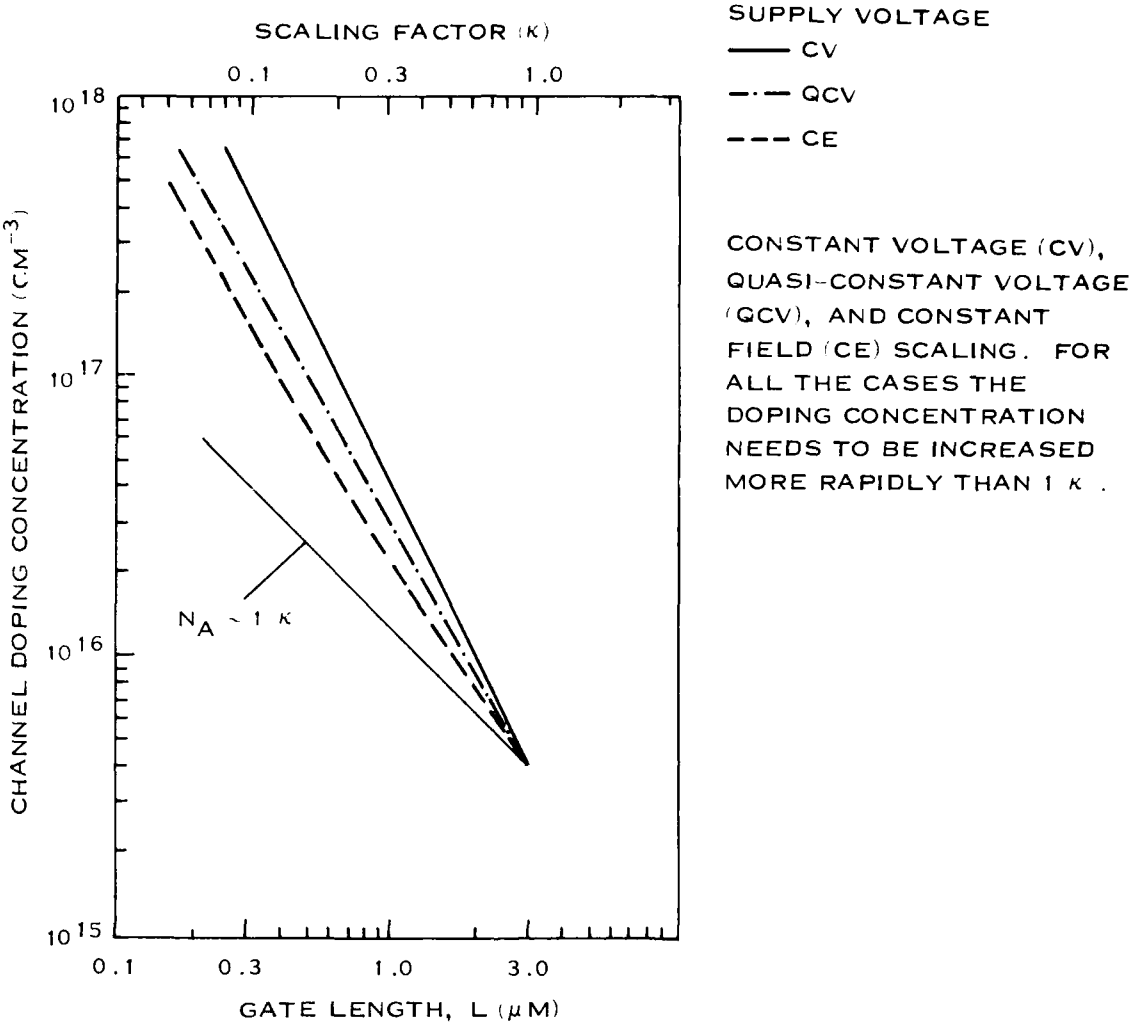


Figure 34. Calculated Channel Doping Concentration Versus Gate Length for Three Different Scaling Scenarios

The last problem can be circumvented by covering the gate polysilicon by oxide (deposited plasma oxide or oxidation), and then lithographically patterning this oxide before the silicide formation as shown in Figure 36(b). This structure, however, does not take full advantage of low resistive silicides because the portion of source/drain region under this lithographically dimensioned oxide is not covered by silicide. An extra mask step is another problem. A self-aligned structure can be realized by anisotropically etching the oxide instead of lithographically defining the gate, leaving a minimal amount of oxide covering the sides of the polysilicon gate.[46] This structure is shown in Figure 36(c). The remaining oxide is referred to as "sidewall" oxide. The source/drain is implanted before the sidewall formation. The last modification is adding very shallow source/drain junctions *before* the sidewall formation. Deeper source/drain junctions are then formed after the sidewall formation, followed by siliciding of source/drain region.[47] The final structure is illustrated in Figure 36(d). These shallow source/drain junctions are formed by a "reachthrough" implant before the oxide deposition. Because the junctions are shallow, the gate/drain

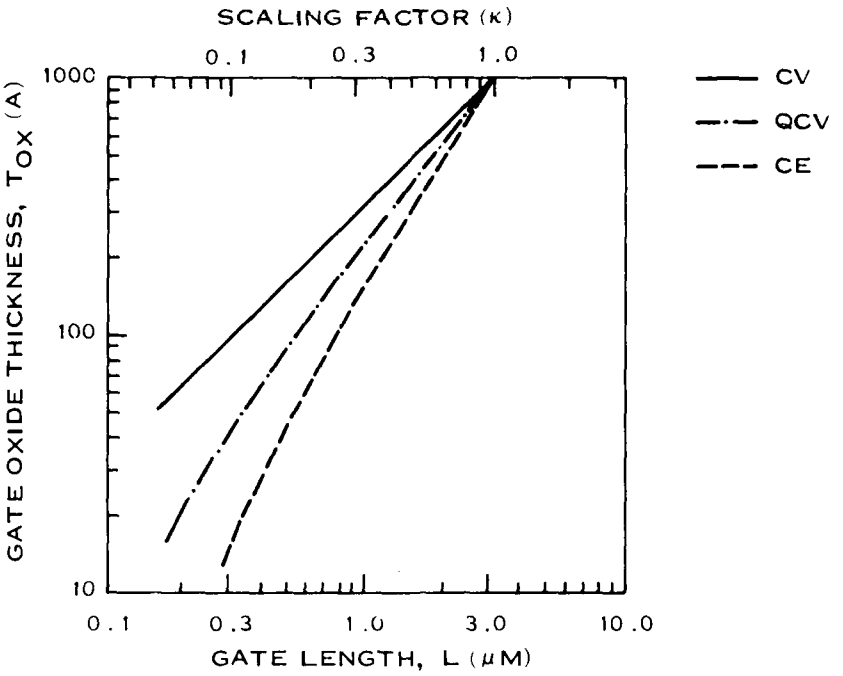


Figure 35. Calculated Gate-Oxide Thickness Versus Gate Length for Three Scaling Scenarios

overlap capacitance is minimal, which is an important requirement for high-speed devices. The short-channel effect is also minimized. All but a small portion, less than a lithographic dimension, of the source/drain junctions is covered by silicide, therefore reducing the parasitic series resistance. Moreover, deep source/drain junctions with high conductance can be used as interconnect lines. Similar structures without silicide on source/drain regions have recently been described by others [48,49] with slight differences in fabrication techniques.

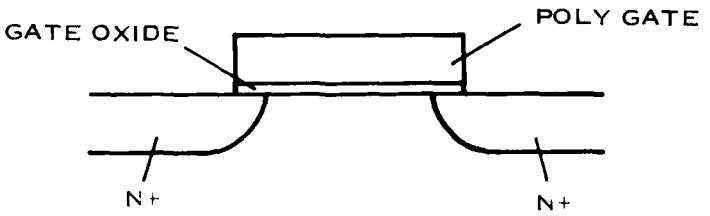
Another advantage of the use of shallow source/drain junctions is that when these junctions are lightly doped, the structure reduces the peak electric field at the drain end by spreading the high electric field into the lightly doped region.[49] As a result, the structure increases breakdown voltage and reduces hot electron effects. This structure is called depletable, or lightly doped drain-source (LDD) structure.[49] With primary and secondary impact ionization being important considerations in designing scaled devices, the structural improvement of this kind seems essential for successful operation of these devices.

[48]W.R. Hunter, T.C. Holloway, P.K. Chatterjee, and A.F. Tasch, Jr., "New Edge-Defined Vertical-Etch Approaches for Submicrometer MOSFET Fabrication," *IEDM Tech. Dig.* (1980) pp. 764–766.

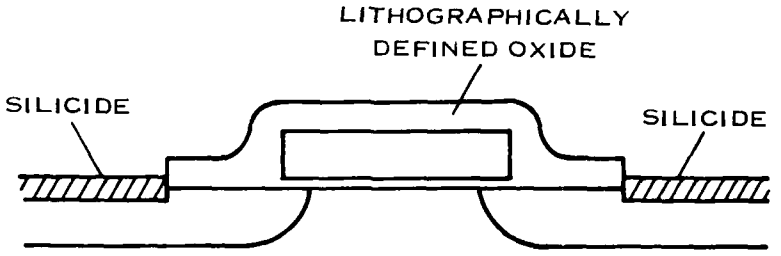
[48]A.F. Tasch, Jr. et al., TI Case No. 7380 (April 10, 1978).

[48]K. Ohta, K. Yamada, M. Saito, K. Shimizu, and Y. Tarui, "Quadruply Self-Aligned MOS (QSA MOS)—A New Short Channel High Speed High-Density MOSFET for VLSI," *IEEE Trans. Electron Devices* **ED-27** (August 1980) pp. 1352–1358.

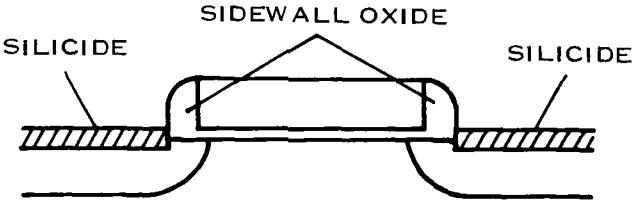
[49]S. Ogura, P.J. Tsang, W.W. Walker, D.L. Critchlow, and J.F. Shepard, "Design and Characteristics of the Lightly Doped Drain-Source (LDD) Insulated Gate Field-Effect Transistor," *IEEE Trans. Electron Devices* **ED-27** (August 1980) pp. 1359–1367.



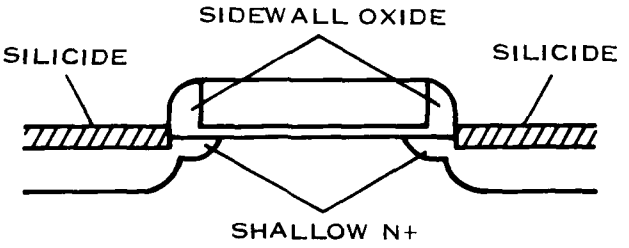
(A) CONVENTIONAL SELF-ALIGNED POLYSILICON GATE MOS STRUCTURE



(B) CONVENTIONAL SELF-ALIGNED POLYSILICON GATE MOS STRUCTURE WITH LITHOGRAPHICALLY DEFINED OXIDE AND SILICIDE ON SOURCE DRAIN (S D) JUNCTIONS



(C) CONVENTIONAL SELF-ALIGNED POLYSILICON GATE MOS STRUCTURE WITH SIDEWALL OXIDE AND SELF-ALIGNED SILICIDE ON S D JUNCTIONS



(D) CONVENTIONAL SELF-ALIGNED POLYSILICON GATE MOS STRUCTURE WITH SIDEWALL OXIDE, SELF-ALIGNED SILICIDE, AND SHALLOW LIGHTLY DOPED "REACHTHROUGH" REGION

Figure 36. Self-Aligned Polysilicon Gate MOS Structure From Unscaled Through Three Variations

D. FACTORS THAT AFFECT DEVICE PERFORMANCE

1. Field-Dependent Mobility

With increasing channel doping and higher electric field strength in scaled devices, the mobility rolloff under high electric field is an important factor in determining the device performance. The mobility of electrons and holes at the Si-SiO_2 interface are affected both by the perpendicular and parallel (to the interface) electric fields.[37] The mobility also decreases with increasing doping as in bulk silicon. However, Sabnis and Clemens have recently shown[11] that the electron mobility is not a function of doping density at higher values of perpendicular fields. Rather, the mobility decrease solely results from the increased perpendicular field experienced by the inversion charge. The higher doping leads to the higher electric field at the interface, which forces carriers closer to the interface. As a result, the increased surface scattering causes a decrease in mobility. The increased impurity scattering has little effect if the carriers are confined to a narrow region at the interface. On the other hand, at relatively low perpendicular fields, the carriers are spread more into the bulk, and an increase in impurity scattering has significant effect.[11] For simplicity, however, we assume that the mobility is only a function of perpendicular and parallel electric fields.

The dependence of mobility on these electric fields, suggested by Thornber,[50] is adopted:

$$\mu(E_\perp, E_\parallel) = \frac{\mu(E_\perp)}{\left\{1 + \left(\frac{E_\parallel}{E_{cy}}\right)^{\beta}\right\}^{1/\beta}} = \frac{\mu_0}{\left(1 + \frac{E_\perp}{E_{cx}}\right)\left\{1 + \left(\frac{E_\parallel}{E_{cy}}\right)^{\beta}\right\}^{1/\beta}} \tag{115}$$

where $E_\parallel$ and $E_\perp$ are the parallel and perpendicular electric fields, respectively, and E_{cx}, E_{cy}, and β are constants. In Equation (115), the explicit dependences of the mobility on $E_\parallel$ and $E_\perp$ are shown, and μ_0 is the low-field mobility independent of $E_\parallel$ and $E_\perp$.

The dependence on the parallel field in Equation (115) is slightly different from the simpler form commonly used,[35,36] which is written as

$$\mu(E_\perp, E_\parallel) = \frac{\mu(E_\perp)}{\left(1 + \frac{E_\perp}{E_{cy}}\right)} \tag{116}$$

Although simple, the use of Equation (116) is not recommended because it underestimates the mobility by a factor of almost 2 at around the transition electric field from low-field to saturation region. $E_\parallel$ is approximately given by

$$E_\parallel = \frac{V_{DS}}{L_{eff}} \tag{117}$$

where V_{DS} is the drain-source voltage, and L_{eff} is the effective channel length. Because of the sidewall oxide, L_{eff} is assumed to be the same as the patterned gate length, L.

[50]K.K. Thornber, "Relation of Drift Velocity to Low-Field Mobility and High-Field Saturation Velocity," *J. Appl. Phys.* **51** (April 1980) pp. 2127–2136.

The perpendicular electric field, $E_\perp$, arises both from the bulk depletion charge, Q_B, and the inversion charge, Q_N. Since the inversion charge is distributed over a certain width (50 ~ 100 nm),[51] the average electric field it experiences from its own charge is $Q_N/2\epsilon_{Si}$. Therefore, the total effective field is

$$E_\perp = \frac{1}{\epsilon_{Si}}\left(Q_B + \frac{1}{2}Q_N\right) \tag{118}$$

Q_B is given by the usual formula

$$Q_B = \sqrt{2\epsilon_{Si}\, qN_A\,(2\phi_f + V_{BS})} \tag{119}$$

and Q_N in the strong inversion region is given by[41]

$$Q_N = C_{ox}(V_{GS} - V_T) \tag{120}$$

where V_{GS} is the gate-source voltage.

Alternatively, considering the electric field at the Si-SiO_2 interface, one can also use

$$E_\perp = \frac{1}{\epsilon_{Si}}(Q_B + Q_N) = \frac{\epsilon_{ox}}{\epsilon_{Si}} \cdot \frac{V_{SG} - V_{FB} - 2\phi_f}{t_{ox}} \tag{121}$$

where V_{FB} is the flat-band voltage and t_{ox} is the gate oxide thickness.

Combining Equations (115), (118), and (120), the perpendicular-field-dependent mobility can also be written as

$$\mu(E_\perp) = \frac{\mu_o}{1 + \theta_o(V_{GS} - V_T) + \dfrac{E_B}{E_{cx}}} \tag{122}$$

where

$$\theta_o = \frac{\epsilon_{ox}}{2\,\epsilon_{si} t_{ox} E_{cx}} \tag{123}$$

and

$$E_B = \frac{Q_B}{\epsilon_{si}} \tag{124}$$

is the electric field of only the bulk depletion charge. Recent experiments[52,53] have yielded $\theta_o = 0.048 \sim 0.064$.

Using resistive-gate MOSFETs, Coen and Muller[37] have determined the values for μ_o, E_{cx}, E_{cy}, and β. Their results, however, are in terms of the electric field at the interface, not the average electric field. We have converted their data in terms of average electric field, and obtained $E_{cx} = 4.2 \times 10^5$ V/cm for <100> electrons, and $E_{cx} = 5.2 \times 10^5$ V/cm for <100> holes. Table 4 summarizes the data by other workers.[11,37,52,53] Some of them are obtained using Equation (123) from the value of θ_o.

[51]F. Stern, "Quantum Properties of Surface Space-Charge Layers," *CRC Crit. Rev. Solid State Sciences* **4** (May 1974) pp. 499–514.

TABLE 4. EXPERIMENTAL VALUES OF E_{cx} AND θ

Reference	Critical Field, E_{cx} (V/cm)	Mobility Reduction Factor, θ
Coen and Muller[37]	4.2×10^5 (electrons)* (7×10^5)	0.045
	5.2×10^5 (holes)* (8.1×10^5)	0.038
Suciu and Johnston[53]	9.1×10^5 (electrons)	0.064
Sabnis and Clemens[11]	4.5×10^5 (electrons)	0.041
Demoulin et al.[52]	6.9×10^5 (electrons)	0.0485

*Recalculated for average electric field
The original values are in parentheses. See the text.

A different empirical formula for the mobility dependence on the perpendicular electric field (and the doping) has been used by Sun and Plummer,[54] which is in the form

$$\mu_{eff} = \frac{\mu_o(N_A)}{1 + \alpha(N_A)\, Q_f} \left(\frac{E_c}{E_{eff}}\right)^{C_1} \tag{125}$$

where N_A is the doping, $\mu_o(N_A)$ is the doping-dependent low field mobility, Q_f is the oxide charge density. E_c is a constant dependent on both N_A and Q_f, E_{eff} is the perpendicular electron field given by (118), and α and C_1 are constants dependent on N_A. Although Equation (125) is a rather different form from Equation (122), both give approximately the same result for a reasonable value of Q_f ($0.5 \sim 1 \times 10^{11}$ cm^{-2}) and are equally applicable. In our calculation we use the relation (122) with the parameters given by Coen and Muller[37] except the previously mentioned correction on E_{cx}. Table 5 summarizes these parameters for surface electrons and holes.

2. Source-Drain Series Resistance

It has been shown[35,36] that the parasitic series resistance associated with an intrinsic MOS device limits the drain current and the gain of the device. This resistance arises from the resistance of the ion-implanted source/drain (S/D) junctions, and the contact resistance between the silicide and ion-implanted junctions (for the silicided S/D) or between metal contact and ion-implanted junctions (for the nonsilicided case). Although a simple one-dimensional analysis is possible to estimate the series resistance for the nonsilicided case, the situation becomes complicated for the silicided case with distributed contact resistance between the silicide and the junction. This is particularly so as the geometry is scaled down because of the larger contribution of contact resistance and because of current crowding.

Recently, Scott, et al.[40] have extended the transmission line model[55,56] to analyze the parasitic series resistance of a silicided source/drain region. Figure 37 shows the device structure (as shown in Figure 36) that is considered, with the notation for the dimensions and the sheet resistivity of each region. The

[52]E. Demoulin, J.A. Greenfield, R.W. Dutton, P.K. Chatterjee, and A.F. Tasch, Jr., "Process Statistics of Submicron MOSFETs, *IEDM Tech. Dig.* (1979) pp. 34–37.

[53]P.I. Suciu and R.L. Johnston, "Experimental Derivation of the Source and Drain Resistance of MOS Transistors," *IEEE Trans. Electron Devices* **ED-27** (September 1980, pp. 1846–1848.

[54]S.C. Sun and J.D. Plummer, "Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces," *IEEE Trans. Electron Devices* **ED-27** (August 1980) pp. 1497–1508.

[55]H. Murrmann and D. Widmann, "Current Crowding on Metal Contacts to Planar Devices," *IEEE Trans. Electron Devices* **ED-16** (December 1969) pp. 1022–1024.

[56]H.H. Berger, "Models for Contacts to Planar Devices," *Solid-State Electron* **15** (1972) pp. 145–158.

TABLE 5. MOBILITY PARAMETERS USED IN THE CALCULATION FOR <100> SILICON

	(cm^{2n}/Vs)	E_{cx} (V/cm)	E_{cy} (V/cm)	β
Electron	850	4.2×10^5	8.7×10^3	2.9
Hole	210	5.2×10^5	1.2×10^4	2.6

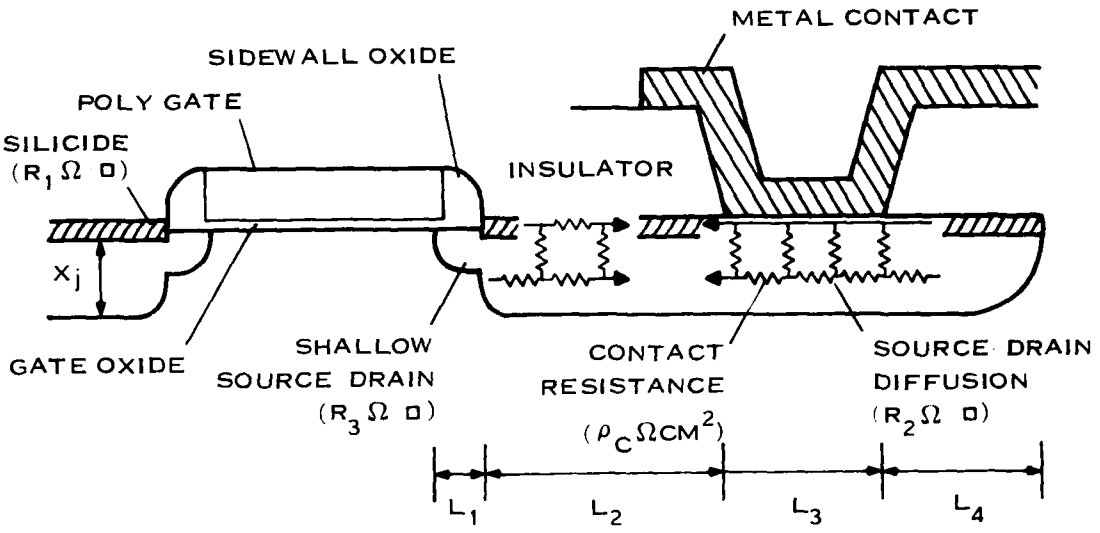


Figure 37. Device Structure, Relative Dimensions and Sheet Resistivity

source and drain are assumed to be symmetric. R_1, R_2, and R_3 are the sheet resistivity of the silicide layer, the ion-implanted junction, and the shallow "reachthrough" region, respectively, and ρ_c denotes the specific contact resistivity between the silicide and the ion-implanted junction. Using their result, the total series resistance can be expressed as[40]

$$R_T = R_3 \frac{2L_1}{W} + \left(\frac{R_1R_2}{R_1R_2}\right)\frac{2L_2}{W} + \frac{2\left\{\frac{R_2^2}{W\beta R_1}\sinh \beta L_2 + \frac{R_c'R_2}{R_1+R_2}\left(2 + \frac{R_1^2+R_2^2}{R_1R_2}\cosh \beta L_2\right)\right\}}{\left\{\frac{R_1+R_2}{R_1}\cosh \beta L_2 + \frac{R_c'}{R_1}\beta W \sinh \beta L_2\right\}} \tag{126}$$

where W is the width of the device, $\alpha = (R_2/\rho_c)^{1/2}$ and $\beta = [(R_1 + R_2)/\rho_c]^{1/2}$. In Equation (126) R_c' is given by

$$R_c' = \frac{R_2}{W\alpha}\frac{\left\{(R_1+R_2)\cosh \alpha L_3 + \frac{R_2\beta}{\alpha}\tanh \beta L_4 \sinh \alpha L_3\right\}}{\left\{(R_1+R_2)\sinh \alpha L_3 + \frac{R_2\beta}{\alpha}\tanh \beta L_4 \cosh \alpha L_3\right\}} \tag{127}$$

R_c' represents the equivalent resistance of sections 3 and 4 (L_3 and L_4), which terminates the right hand side of section 2 (L_2). The first two terms in Equation (126) are simply line resistances of section 1 (L_1) and section 2 (L_2), while the third term is identified as the contact resistance. One can obtain a similar result for a nonsilicided case if one sets $L_2 = L_4 = 0$ in the contact resistance term and if the second term of Equation (126) is replaced by $2R_2L_2'/W$ where L_2' is the length of the nonsilicided, ion-implanted junction, and ρ_c in this case represents the specific contact resistivity between metal contact and the junction. Note that Equation (126) then reduces to

$$R_c' = \frac{R_s}{W\alpha} \cosh \alpha L_3 \tag{128}$$

which is the expression for contact resistance derived by Berger.[56]

Equations (126) and (127) are used to examine how the parasitic series resistance scales. First of all, the scaling property of the sheet resistance of ion-implanted junctions, as the junction depth, x_j, is decreased, is considered. In the past[34,35] the $1/x_j$ dependence of sheet resistivity has been extensively used. This dependence, however, is only valid for a relatively deep junction that can maintain a doping concentration close to solid solubility throughout most of its depth. To obtain a very shallow junction, the peak doping concentration needs to be reduced so that the initial depth after ion implantation and the diffusion during annealing are minimized. This reduction of peak concentration results in a much more rapid increase in sheet resistivity.

To illustrate the dependence of sheet resistivity on junction depth, Figure 38 shows the results from SUPREM[57] simulations of arsenic and boron implanted junctions that have been subsequently driven in during annealing. The arsenic junction simulation has used a 10-keV implant and annealing at 950°C for 20 minutes to obtain high carrier concentration even for the highest dose (1×10^{16} cm^{-2}).[58] The boron junction simulation has used a boron implant at 10 keV through 100 nm of oxide, annealed at 900°C for 50 minutes. This annealing condition is sufficient to activate implanted borons for all the doses.[59,60] For both types, the implant dose has been adjusted to obtain a specified junction depth with fixed annealing conditions. The junction depth is defined by the depletion edge of the junction with zero applied voltage.[38] From Figure 38 one can see a much stronger dependence of sheet resistivity on junction depth than $1/x_j$, which is shown for a comparison by a broken curve. For the boron diffused junction, the sheet resistivity, R_D, can be closely approximated by

$$R_D = k_1\left(\frac{1}{x_j}\right)^6 \tag{129}$$

where $k_1 = 0.8\ \Omega\ \mu m^6$, R_D is in Ω/sq, and x_j in micrometers. Similarly, for the arsenic diffused junction, the variation can be expressed as

$$R_D = k_2\left(\frac{1}{x_j}\right)^5 + k_3\left(\frac{1}{x_j}\right) \tag{130}$$

[57]D.A. Antoniadis and R.W. Dutton, "Models for Computer Simulation of Complete IC Fabrication Process," *IEEE Trans. Electron Devices* **ED-26** (April 1979) pp. 490–500.

[58]M.Y. Tsai, F.F. Morehead, J.E.E. Baglin, and A.E. Michael, "Shallow Junctions by High-Dose As Implants in Si: Experiments and Modeling," *J. Appl. Phys.* **51** (June 1980) pp. 3230–3235.

[59]F. Schwettmann, "Evaluation of Boron Implanted Layers in Silicon," Texas Instruments Technical Report, No. 03–72–89 (June 1972).

[60]M.Y. Tsai, "Studies of High-Dose Ion Implantation in Silicon," Ph.D. Thesis, University of Illinois (September 1978).

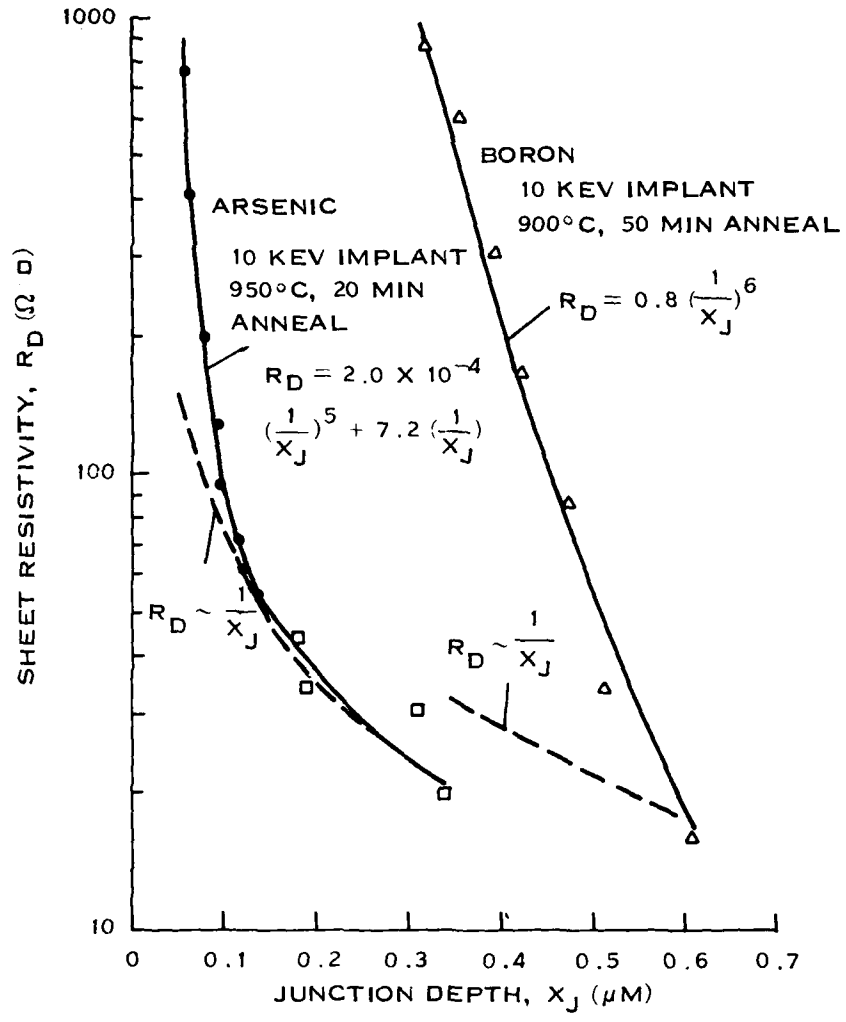


Figure 38. SUPREM Simulation of Sheet Resistivity Versus Junction Depth for Boron and Arsenic Junctions

where $k_2 = 2.0 \times 10^{-4}\ \Omega\ \mu m^5$, and $k_3 = 7.2\ \Omega\ \mu m$. For arsenic, the sheet resistivity varies as $1/x_j$ down to $\sim 0.1\ \mu m$, below which the resistivity starts to increase quite rapidly as the junction depth is decreased further. Therefore, the $1/x_j$ dependence previously assumed gives an overly optimistic picture of scaled-down junctions. The larger junction depth for boron as shown in Figure 38, arises from deeper penetration of boron during implant because of its lighter mass compared to arsenic and also from the higher diffusion coefficient of boron.

The decrease in peak doping concentration of the implanted junction causes another problem in scaled devices. The specific contact resistivity, ρ_c, of metal-semiconductor contacts depends strongly on the doping concentration of the semiconductor, and a rapid increase of ρ_c is anticipated as the junction depth is decreased. Blair et al.[61] have measured the specific contact resistivity of PtSi on boron and

[61]J.C. Blair, C.R. Fuller, and P.B. Ghate, "Platinum-Silicide Contacts," Texas Instruments Technical Report, No. 03-74-91 (April 1974).

phosphorus junctions as a function of surface concentration. We have combined their results with the results from the SUPREM simulation to relate the surface concentration to the implant dose and, therefore, to relate the specific contact resistivity to the junction depth, x_j. For a boron junction, the resulting relation is approximately expressed as

$$\rho_c = 1.33 \times 10^{-3} \times \exp\left(-\frac{x_j}{0.0637}\right) \tag{131}$$

where x_j is in units of micrometers, and ρ_c is in $\Omega\ \text{cm}^2$. The strong dependence of ρ_c on the junction depth is obvious. No data was available on the corresponding dependence for arsenic junctions, and we used Blair's data[61] on phosphorus junction to estimate the dependence for arsenic junction and obtained $\rho_c = 4.4 \times 10^{-4} \times \exp(-x_j/0.011)$. The specific contact resistivity of an arsenic junction is expected to be larger than that of a boron junction because of the larger Schottky barrier height. Although these relations are obtained for a specific silicide (PtSi), they are sufficient to obtain a first-order estimate of the specific contact resistivity.

As described in Subsection C, the shallow reachthrough source/drain region should be lightly doped. The low doping results in high sheet resistivity of this region. With the siliciding of the source/drain region, this highly resistive region is expected to constitute most of the parasitic series resistance. However, as the channel doping concentration is increased by scaling, the doping concentration of this shallow S/D region also needs to be increased and, therefore, the resistance is expected to decrease. The SUPREM simulation[57] has shown that the relation between the sheet resistivity (R_3) and the implant dose (N_D) of this region can be described approximately as (Reference 49)

$$R_3 = 8.84 \times 10^3\ (N_D/1 \times 10^{12})^{-0.569} \tag{132}$$

where R_3 is in units of Ω/sq, and N_D is cm^{-2}. Assuming that the implant dose must be five times higher than the channel implant dose, the sheet resistivity can be related to the channel doping concentration as

$$R_3 = 7.70 \times 10^3\ (N_4/1 \times 10^{16})^{-0.569} \tag{133}$$

where R_3 is in Ω/sq, and the channel doping concentration, N_4, is in units of cm^{-3}.

There is some doubt about the validity of using shallow source/drain junctions for p-channel devices because it is extremely difficult to obtain a boron junction depth less than 0.3 μm. In addition, with smaller probability of hole impact ionization at the drain end,[35] it may not be necessary to have a lightly doped region. Therefore, no distinction has been made in our analysis between shallow and deep source/drain regions for a p-channel device.

The sheet resistivity of the silicide, R_1, is assumed to be constant. R_1 depends on the thickness of the silicide, which tends to be scaled down with other dimensions. The silicide thickness, however, should be held maximum to accommodate higher current density.

In Subsection E, the equations (126) through (133) will be used to calculate the parasitic series resistance of a scaled device.

3. Finite Inversion Layer Thickness

When the channel length of an MOS device is scaled down, the gate oxide thickness must also be scaled down as described in Subsection B. Eventually, the gate oxide thickness becomes comparable to the inversion layer thickness, which is estimated to be 30 ~ 100 nm.[51] Then, the potential drop across the inversion layer begins to become comparable to the potential drop across the gate oxide, therefore, causing a saturation of effective gate capacitance. This saturation of gate capacitance causes a degradation of drain current and transconductance.[62]

[61]F. Stern, "Self-Consistent Results for N-Type Si Inversion Layers," *Phys. Rev. B* 5 (June 1979) pp. 4891–4899.

TABLE 6. DEVICE PARAMETERS FOR UNSCALED (κ = 1) MOSFET

Gate length, L	3 μm
L_1	0.3 μm
L_2, L_3, L_4	3 μm
Width, W	15 μm
Junction depth, x_j	0.6 μm
Sidewall oxide thickness	0.3 μm
Supply voltage, V_{DD}	5 V
Threshold voltage, V_T	1 V
Channel doping, N_A	4×10^{15} cm^3
Gate oxide thickness, T_{ox}	900 nm

Although in an actual MOS device the inversion charge is spread over a distance of 50 ~ 200 nm (which is approximately twice the average inversion layer thickness), a simplified model can assume that all of the charge is at a constant distance from the Si–SiO_2 interface. We take this distance to be an average inversion layer thickness, x_{av}. Then, the capacitance of this charge is given by

$$C_{ch} = \frac{\epsilon_{si}}{x_{av}} \tag{134}$$

x_{av} can be estimated from the results of quantum mechanical calculations[51,62] and is approximately expressed as

$$x_{av} = 1.85 \times 10^{-9} \left(Q_B + \frac{1}{3} Q_n \right)^{-1/3} \tag{135}$$

where Q_B and Q_n are given by Equations (119) and (120), respectively, and x_{av} is in units of cm. The effective gate capacitance, C_{eff}, is a series combination of C_{ch} and C_{ox}, which is given by

$$\frac{1}{C_{eff}} = \frac{1}{C_{ch}} + \frac{1}{C_{ox}} \tag{136}$$

Because of the difference in dielectric constant between silicon and SiO_2, the effect of finite inversion layer thickness is negligible until the oxide thickness is less than 100 nm. We have compared our result with the estimate by El-Mansy.[36] His result seems to overestimate the effect of the inversion layer capacitance by a factor of 2 to 3, possibly because of his overestimation of the inversion layer thickness.

E. DEVICE PERFORMANCE

Based on the structural considerations of Subsection C, and the scaling scenarios of Subsection B, the device parameters for an unscaled (κ = 1) device are defined in Table 6. All the horizontal dimensions and the junction depth are assumed to scale down linearly with the scaling factor, κ. The scaling of voltages, doping, and gate oxide thickness has been described in Subsection B. Of interest is the device performance of a scaled device. In particular, the variation of the triode gain and the drive capability as the device dimension is scaled down is examined.

1. Triode Gain

The triode gain of an MOS device can be written as[35]

$$\beta = \frac{\mu C_{eff} \frac{W}{L_{eff}}}{1 + \mu C_{eff} \frac{W}{L_{eff}} R_I (V_G - V_T)} \tag{137}$$

where C_{eff} is the effective gate capacitance given by Equation (136), μ is the field-dependent carrier mobility given by Equation (115), and R_I is the total parasitic series resistance given by Equation (126). R_I acts in a feedback mechanism to reduce the actual voltage below applied terminal voltages and, therefore, reduces the effective triode gain. The drain-source voltage, V_{DS}, in Equation (117) was arbitrarily chosen as

$$V_{DS} = 0.01 (V_G - V_T) \tag{138}$$

to describe the device operation in the linear region. The triode gain is calculated as a function of gate length, or scaling factor, for the three different scaling scenarios described earlier.

The result of the calculation is shown in Figure 39 for n- and p-channel devices, in which the normalized gain

$$K' = \frac{\beta}{2} \frac{L}{W} \tag{139}$$

is plotted as a function of patterned gate length, L. A set of curves for each scaling scenario represents the best and worst cases of series resistance: the upper curve corresponds to the silicided source/drain with very low sheet resistivity ($R_I = 0\ \Omega/\square$), and the lower curve corresponds to the nonsilicided source/drain. For n-channel devices, the gain peaks around 0.3 ~ 0.4-μm gate length for the silicided case, and 0.4 ~ 0.5-μm gate length for the nonsilicided case. The gain improvement by siliciding the source/drain is approximately a factor of 2 to 4. For p-channel devices, the gain peaks at a much larger channel length, 1.2 ~ 1.3 μm for the silicided case, and 1.3 ~ 1.6 μm for the nonsilicided case. For both cases, the constant field scaling (CE) gives the highest gain for a given gate length, and the constant voltage scaling (CV) gives the lowest gain. The peak in gain also shifts to a shorter gate length for constant field scaling. This illustrates the necessity to reduce the operating voltages in scaled technology to obtain the highest possible device performance. In the present MOS technology, the supply voltages are scaled down much slower than the physical device dimensions.

To identify the factors that cause the decrease in triode gain beyond the peak as shown in Figure 39, we need to examine each factor in more detail. For example, Figure 40 shows the mobility variation with the scaling factor for n- and p-channel devices under the operating condition $V_G = 5\ V_T$. Under this condition, the perpendicular electric field, which causes the mobility degradation, results from both the inversion charge and the bulk depletion charge. Because of the small drain-source voltage in the linear region, the velocity saturation effect is negligible in this operation mode. As shown in Figure 40, the mobility in both n- and p-channel devices decrease quite rapidly as the device is scaled down. To see the effect of higher doping concentration in scaled devices, Figure 41 shows the mobility variation under the condition $V_G = V_T$. Under this condition the mobility degradation is only caused by the electric field from the bulk depletion charge, which increases with higher channel doping. As seen in Figure 41, the mobility decreases almost by a factor of 2 as the device is scaled down from 3-μm to 0.3-μm gate length.

Figure 42 shows the variation of parasitic source/drain series resistance with scaling factor for n- and p-channel devices. The cases shown are for a nonsilicided source/drain and silicided source/drain with $R_I = 1\ \Omega$/sq. A surprisingly rapid increase of series resistance for both types is especially noted. For a

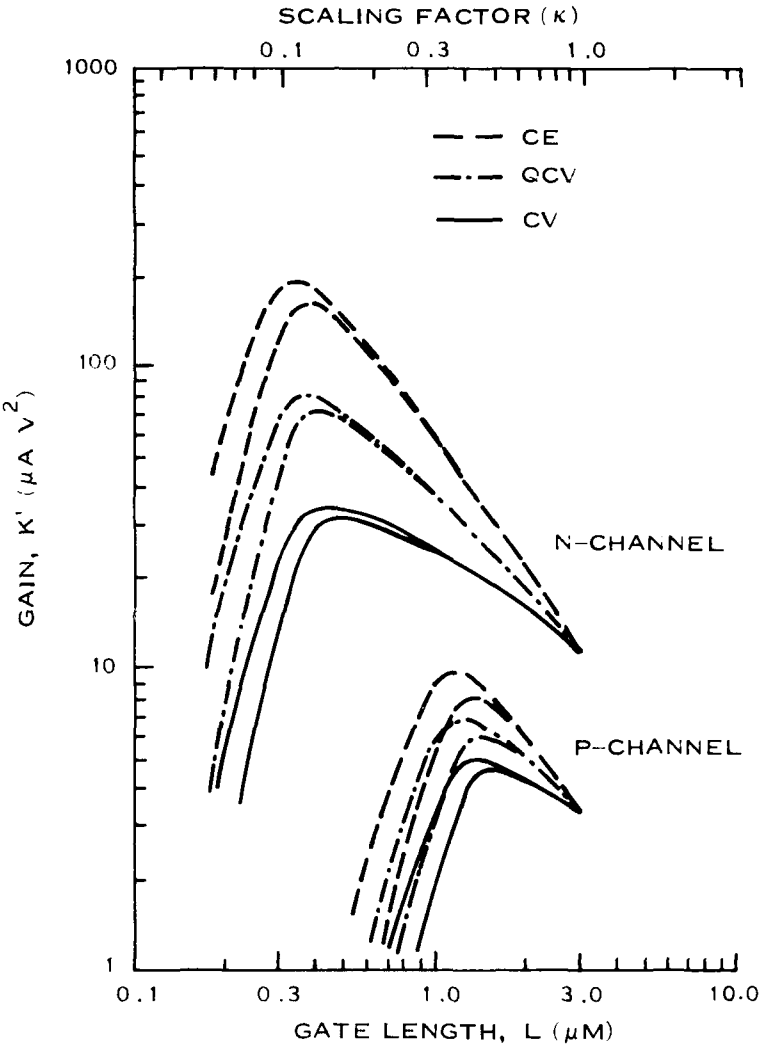


Figure 39. Calculated Triode Gain of N-Channel and P-Channel Devices Versus Gate Length for Three Different Sealing Scenarios of Supply Voltage

p-channel device, this rapid increase is attributed to the increasing sheet resistivity of implanted junctions for the nonsilicided case, and the increasing specific contact resistivity for the silicided case. As explained in the previous section, the increase of contact resistivity results from a decrease in peak doping concentration at the metal-semiconductor interface. To illustrate the rapid increase of specific contact resistivity. Figure 43 shows the variation of specific contact resistivity with scaling factors for n- and p-channel devices using Equations (130) and (131). It should be noted that even for a p-channel device with silicide, a part of the source/drain region under the sidewall oxide is still nonsilicided, which contributes a considerable part to the total series resistance because of the high sheet resistivity of implanted junctions.

The increase of series resistance for an n-channel device with scaling from 3-μm gate to submicron gate length as shown in Figure 42 is a result of increasing sheet resistivity of the lightly doped shallow source/drain region as channel doping is increased for scaled devices. This may be misleading because for

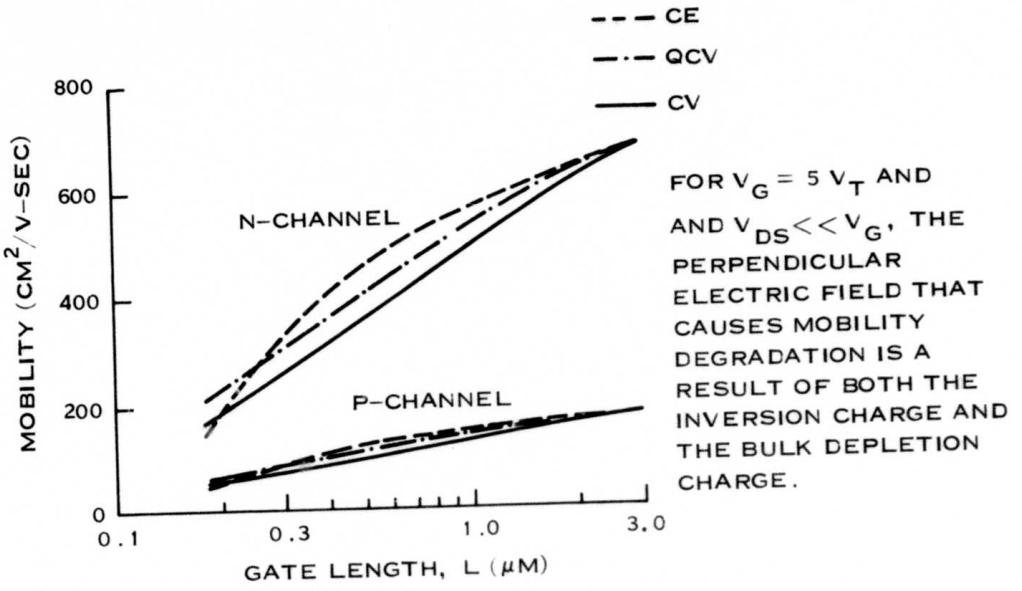


Figure 40. Calculated Surface Carrier Mobility in N-Channel and P-Channel Devices Under Operating Conditions $V_G = 5\ V_T$ and $V_{DS} \ll V_G$

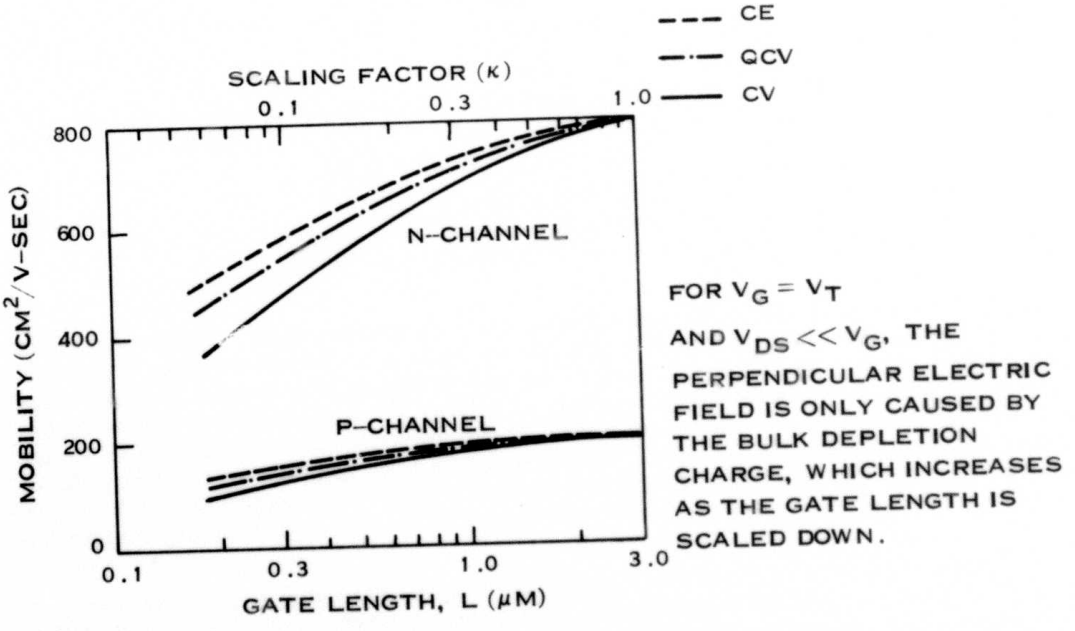


Figure 41. Calculated Surface Carrier Mobility in N-Channel and P-Channel Devices Under Operating Conditions $V_G = V_T$ and $V_{DS} \ll V_G$

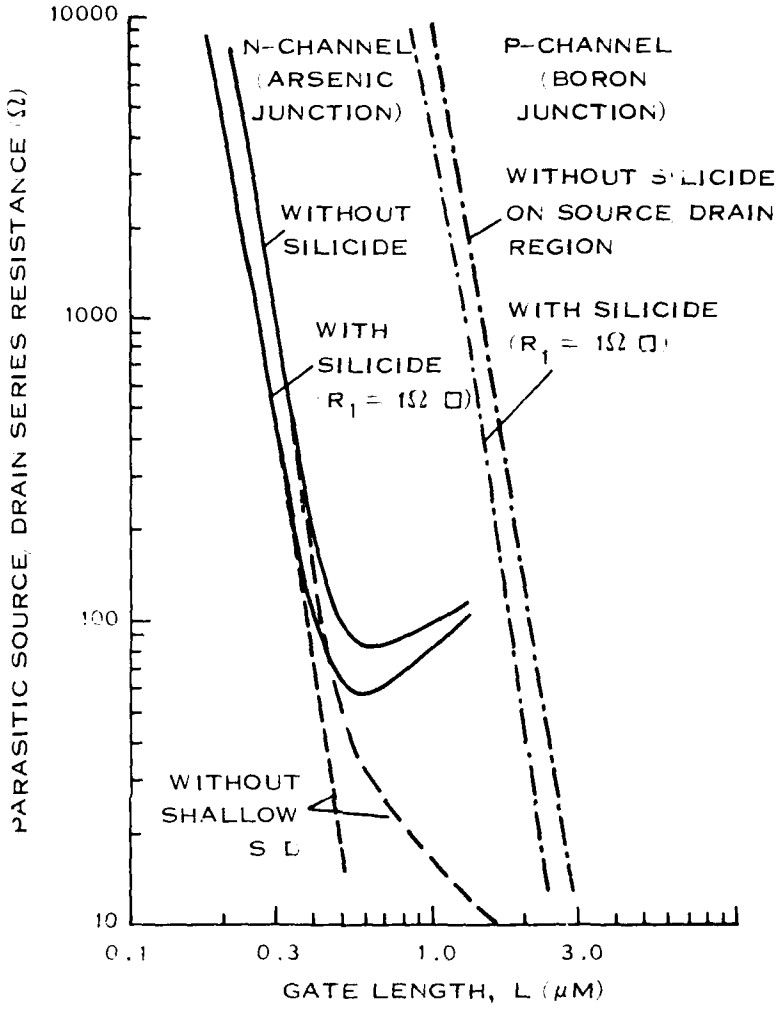


Figure 42. Variation of Parasitic Source/Drain Series Resistance With Gate Length for N-Channel and P-Channel Devices

large device (e.g., above 1-μm gate length) the lightly doped region is unnecessary. Considering that the specific contact resistivity is rather low for an n-channel device ($2 \times 10^{-6}\ \Omega\ cm^2$ at 0.3-μm gate as shown in Figure 43), and that for a silicided case, the only nonsilicided region is the lightly doped source/drain where sheet resistivity decreases, the rapid increase of total parasitic resistance for an n-channel device as shown in Figure 42 may seem puzzling. This increase is related to the notion of current crowding effect and "the critical length" described by Scott et al.[40] In a silicided diffusion structure, the current flows mostly in the low resistive silicide except at the region close to the current source where the current is forced from the silicide into the diffusion. The size of this region is determined by "the critical length" defined by[40]

$$L_c = \sqrt{\frac{\rho_c}{R_1 + R_2}} \tag{140}$$

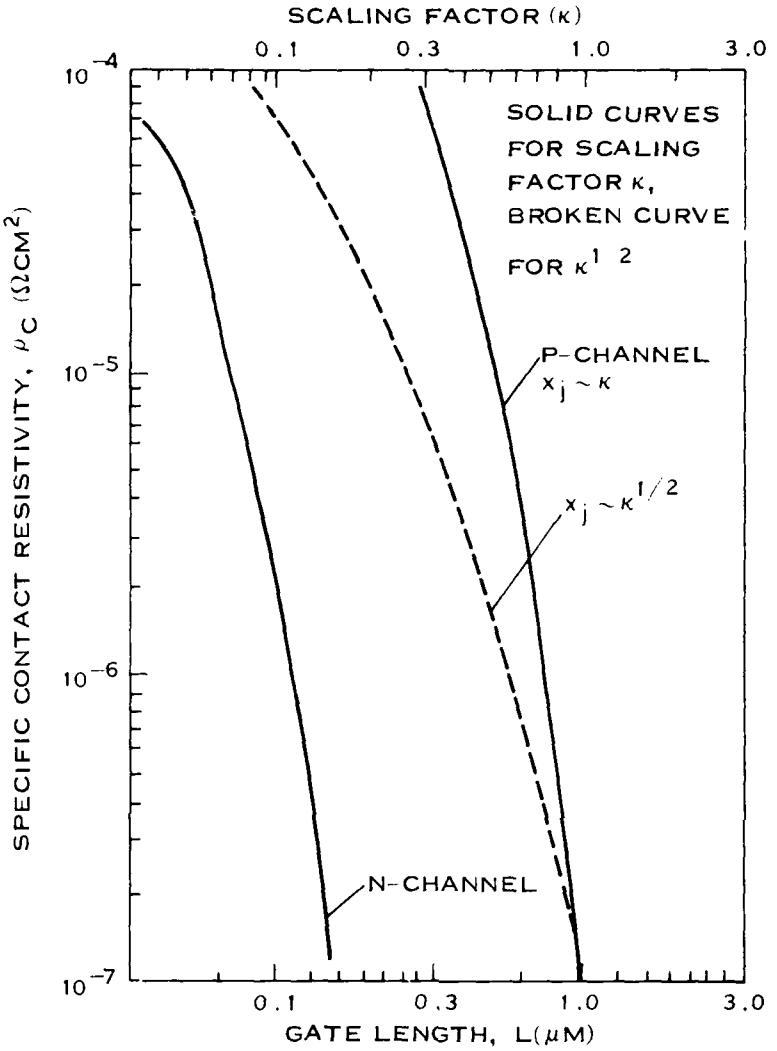


Figure 43. Calculated Specific Contact Resistivity Versus Gate Length for N-Type and P-Type Junction Depths Scaled Linearly

where ρ_c is the specific contact resistivity, and R_1 and R_2 are the sheet resistivities of the silicide and the diffusion, respectively. When the structure size becomes smaller than L_c, the current is no longer confined in the silicide, and the merit of silicided diffusion is lost. The contact resistance then increases quite rapidly as the structure length is reduced. This notion is borne out by Figure 44, which shows the variation of critical length, L_c, for n- and p-channel devices as the feature size is scaled down. For an n-channel device, the size of the silicided region (which has the same length as the gate) actually becomes smaller than L_c, leading to a rapid increase of contact resistance. As shown in Figure 42, for a p-channel device the critical length stays small because of much higher sheet resistivity of diffusion (R_2).

2. Saturation Current

The saturation current of a MOSFET is one of the most important parameters that determine the circuit performance of scaled devices. Because of the high perpendicular electric field involved, we define

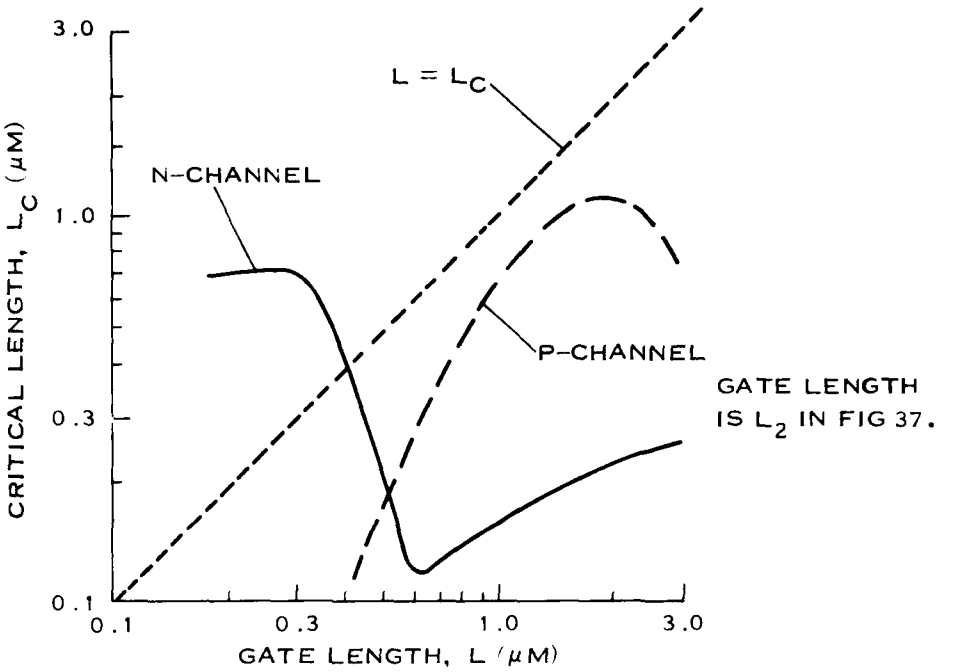


Figure 44. Critical Length Versus Gate Length for N-Type and P-Type Junctions

the saturation drain voltage as the voltage at which the carriers in the inversion layer reach saturation drift velocity.[35] Then, the saturation drain voltage is approximately written as[35]

$$V_{DSAT} = L_{eff}\,E_{cy}\left\{\left[1 + \frac{2}{L_{eff}\,E_{cy}}\left(V_{GS} - V_{FB} - 2\phi_f - F_s\frac{2\epsilon qN_A}{C_{ox}}\sqrt{V_{GS} - V_T + V_{bi}}\right)\right]^{1/2} - 1\right\} \tag{141}$$

Here F_s is the charge-sharing factor[63] at saturation, which is a fraction of the total bulk charge within the channel region. The drain current at $V_{DS} = V_{DSAT}$ is given by

$$I_{DSAT} = \frac{W}{L_{eff}}\mu C_{ox}\left\{\left(\frac{V_{GS} - V_{FB} - 2\phi_f - V_{DSAT}}{2}\right)V_{DSAT}\right.$$
$$\left. - \frac{2}{3}F_s\frac{\sqrt{2\epsilon_{si}qN_A}}{C_{ox}}\left[(V_{DSAT} + V_{BS} + 2\phi_f)^{3/2} - (V_{BS} + 2\phi_f)^{3/2}\right]\right\} \tag{142}$$

where the mobility, μ, is calculated by Equation (115) with the parallel electric field given by

$$E_{\parallel} = V_{DSAT}/L_{eff} \tag{143}$$

[63]P.K. Chatterjee, and J.E. Leiss, "An Analytic Charge-Sharing Predictor Model for Submicron MOSFETs," *IEDM Tech. Dig.* (1980) pp. 28–33.

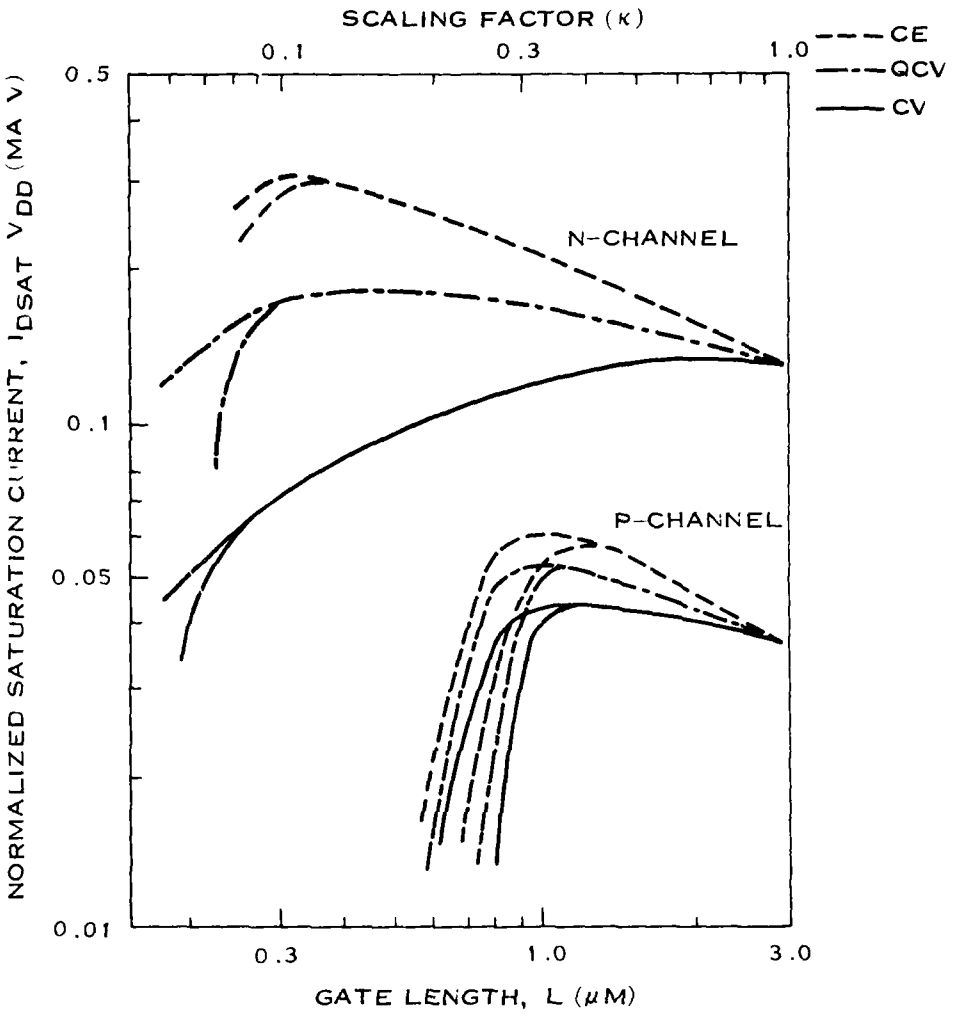


Figure 45. Normalized Drain Saturation Current of N-Channel and P-Channel Devices for Three Scaling Scenarios

to represent the device operation in saturation region. The effect of parasitic series resistance is included as

$$V_{GS} = V'_{GS} - I_{DSAT} R_s \tag{144}$$

Where R_s is the source series resistance, and V'_{GS} is the external gate voltage. Equations (141) to (144) are solved self-consistently by an iterative method to obtain the saturation drain voltage. The threshold voltage change caused by the change in V_{BS} has been neglected.

Figure 45 shows the result of the calculation for n- and p-channel devices. The results are shown in terms of normalized saturation current, I_{DSAT}/V_{DD}. A set of curves for each scaling scenario again indicates the best and the worst cases of series resistance. Large differences between the different scaling scenarios for an n-channel device as seen in Figure 45 is the result of velocity saturation under large parallel electric

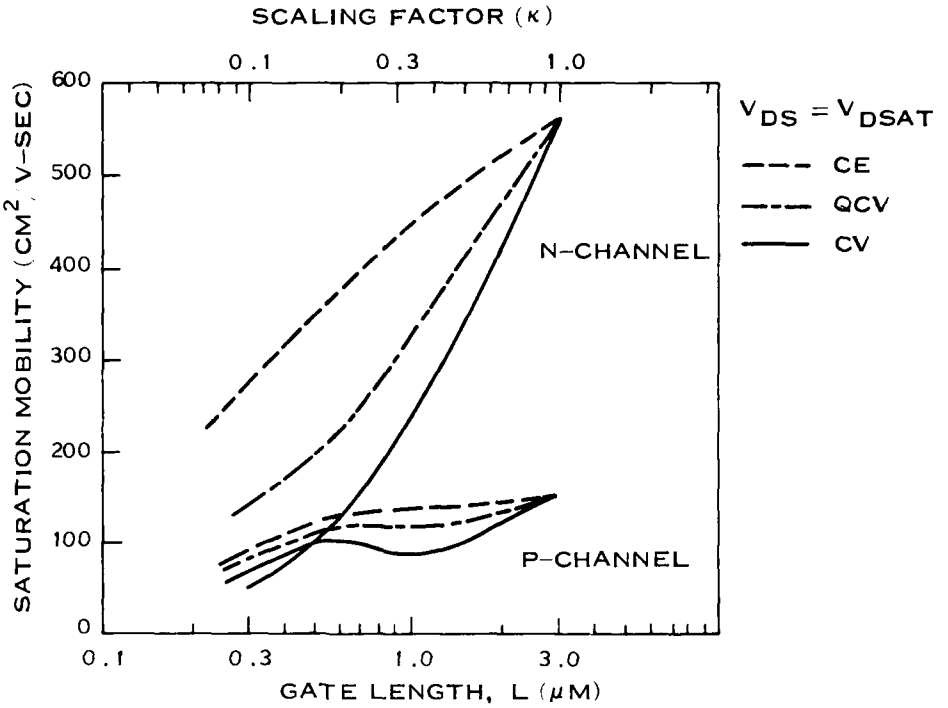


Figure 46. Variation of Calculated Saturation Mobility Versus Gate Length in N-Channel and P-Channel Devices

fields. The effect is largest for constant voltage scaling because of the large electric field involved. Under constant field scaling, the drive current (or drain saturation current) reaches a maximum at a gate length of $\sim 0.3\ \mu m$, which coincides with the peak in triode gain as shown in Figure 39. Comparing two sets of curves in Figure 45, we note that the effect of velocity saturation is smaller for a p-channel device because of the larger critical field for the saturation. The curves for the p-channel device show a trend similar to that shown for the triode gain in Figure 39. It should also be noted that with the parasitic series resistance serving as a feedback factor, the degree of series resistance effect depends on the current level for a given value of the series resistance.

To further illustrate the effect of velocity saturation, Figure 46 shows the saturation mobility (carrier mobility at saturation) for n- and p-channel devices as a function of gate length. Here again, the distinction between n- and p-channel is clear. It further shows the need to reduce the operation voltages to maximize the drive capability with a minimal velocity saturation effect.

F. DISCUSSION

1. Relative Contribution of Higher Order Effects on Device Performance Degradation

Based on the calculations described in the previous section, this section covers the relative contributions of the various parasitic effects on the performance degradation of n- and p-channel scaled devices. To identify the major causes of performance degradation, we start with an "intrinsic" device without any parasitic effects of series resistance such as the diffusion and the contact resistance, inversion layer capacitance, and mobility degradation from perpendicular and parallel (velocity saturation) electric fields. Each parasitic effect is then added separately, and the device performance parameters are calculated. The

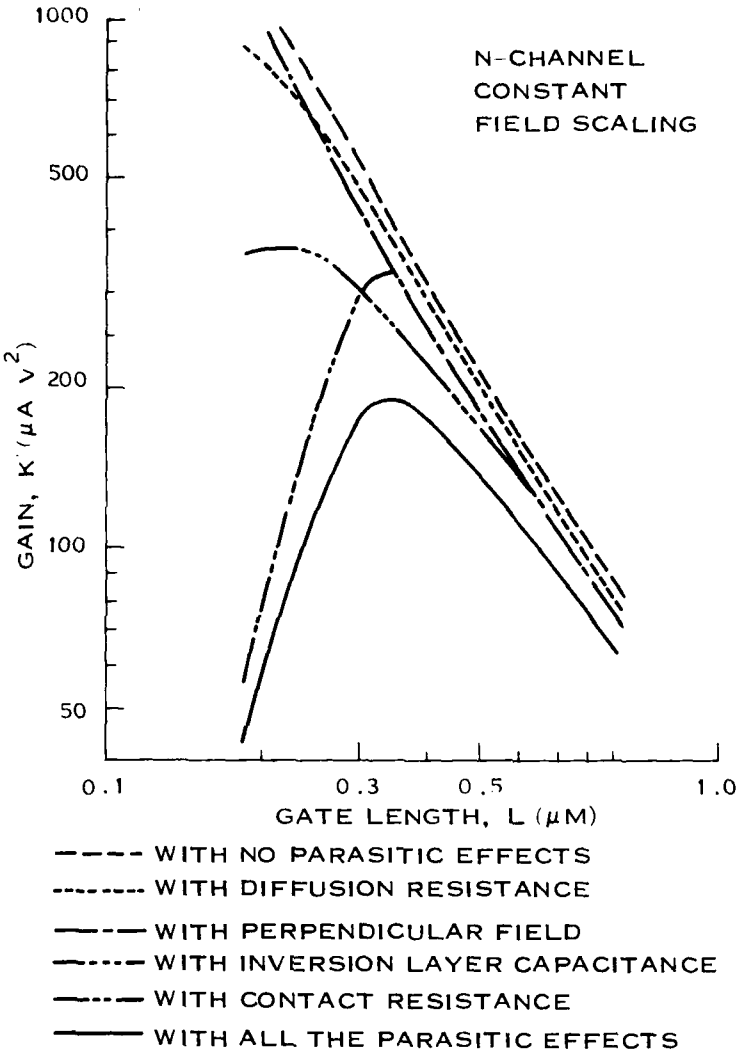


Figure 47. Variation of N-channel Triode Gain Versus Gate Length With Each Parasitic Effect Added Separately

result for triode gain is shown in Figures 47 and 48 for n- and p-channel devices, respectively, for the constant field scaling scheme. The result for an n-channel device (Figure 47) shows the importance of contact resistance below 0.3-μm gate length, whereas the result for p-channel (Figure 49) shows the degradation from both contact resistance and the resistance of the source/drain diffusions below 1 μm. These results have been obtained assuming silicided source/drain with a silicide sheet resistivity of 5 Ω/sq. Note, however, that for a p-channel device a part of the source/drain under the sidewall oxide is still not silicided. A similar result for the drain saturation current is shown in Figures 49 and 50. The general feature is the same as the triode gain except for a relatively large contribution of velocity saturation effect, especially for an n-channel device.

From these calculations we can examine the relative contribution of each parasitic effect on the performance degradation. For example, for the triode gain calculation, we can define the degradation factor, η, for each parasitic effect, by $K' = K_o'/(1 + \eta)$, where K_o' is the gain with no parasitic effects, and K' is the gain when the particular parasitic effect is added. By comparing the degradation factors among

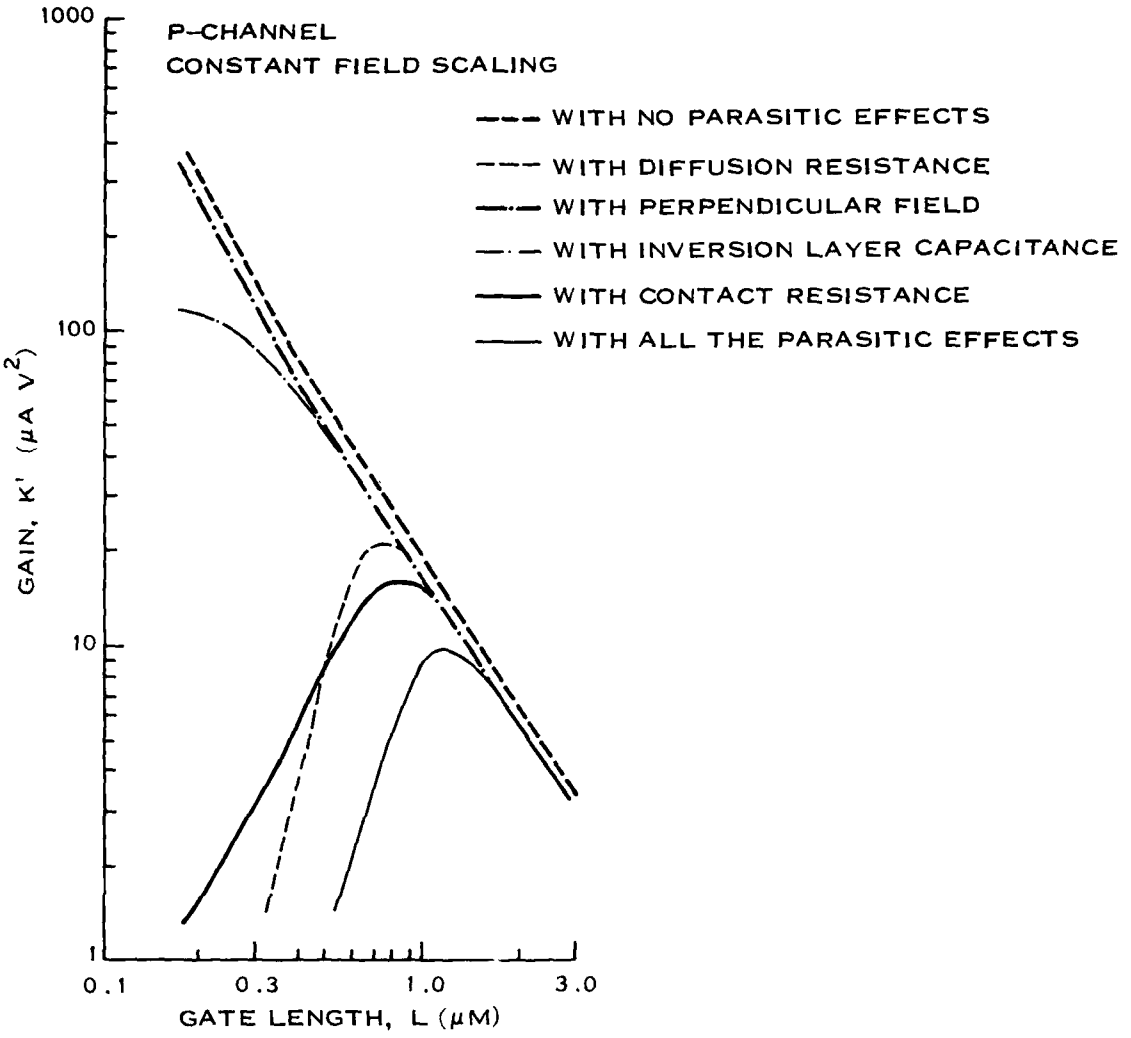


Figure 48. Variation of P-Channel Triode Gain Versus Gate Length With Each Parasitic Effect Added Separately

all the parasitic effects, the relative contribution is identified. Figures 51 to 54 show the result for the triode gain and the drain saturation current under constant field and constant voltage scaling scenarios. These figures illustrate semi-quantitatively the relative importance of the parasitic effects as the device is scaled down from 3 μm gate length. It should be cautioned that, comparing Figures 47 to 50 and Figures 51 to 54, the overall (combined) degradation factors increase for smaller gate length in all the cases, and that what is shown in Figures 51 to 54 is the relative, not absolute, contribution. For example, in Figure 51 the decrease in diffusion resistance contribution does not mean the decrease in actual diffusion resistance.

Comparing Figures 51 and 52, a relatively large degradation from the perpendicular electric field in both cases is noticed. This is a result of the heavy doping of the channel region to reduce the short-channel effect and to avoid the punchthrough. This degradation can be minimized by shallow implant of

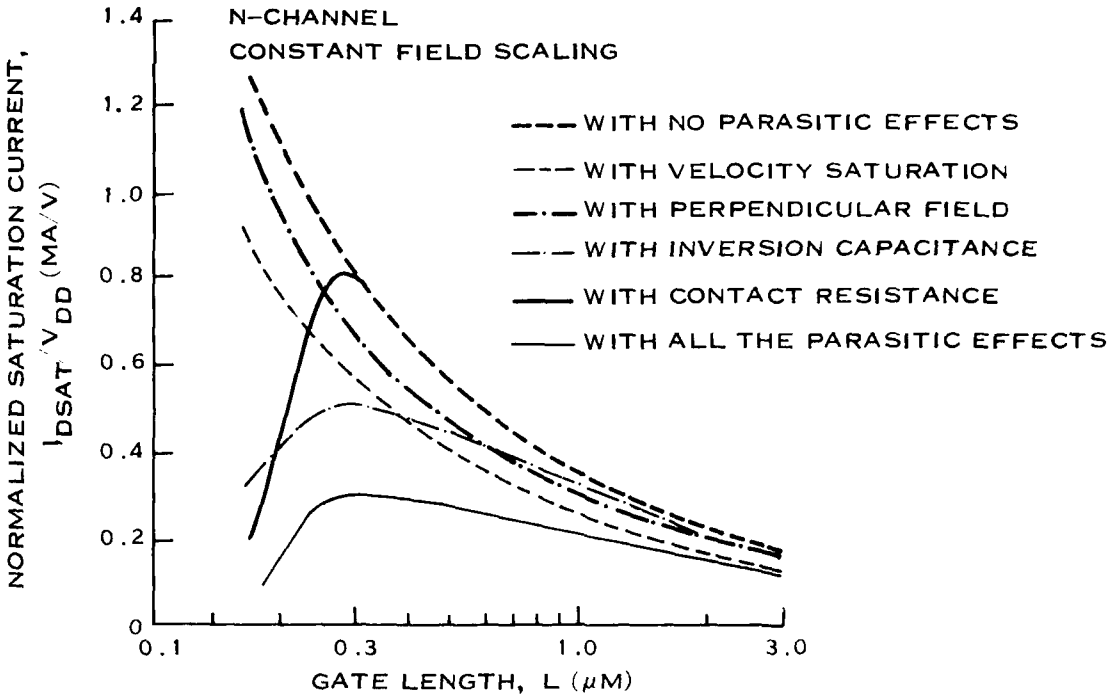


Figure 49. Variation of N-Channel Normalized Saturation Current Versus Gate Length With Each Parasitic Effect Added Separately

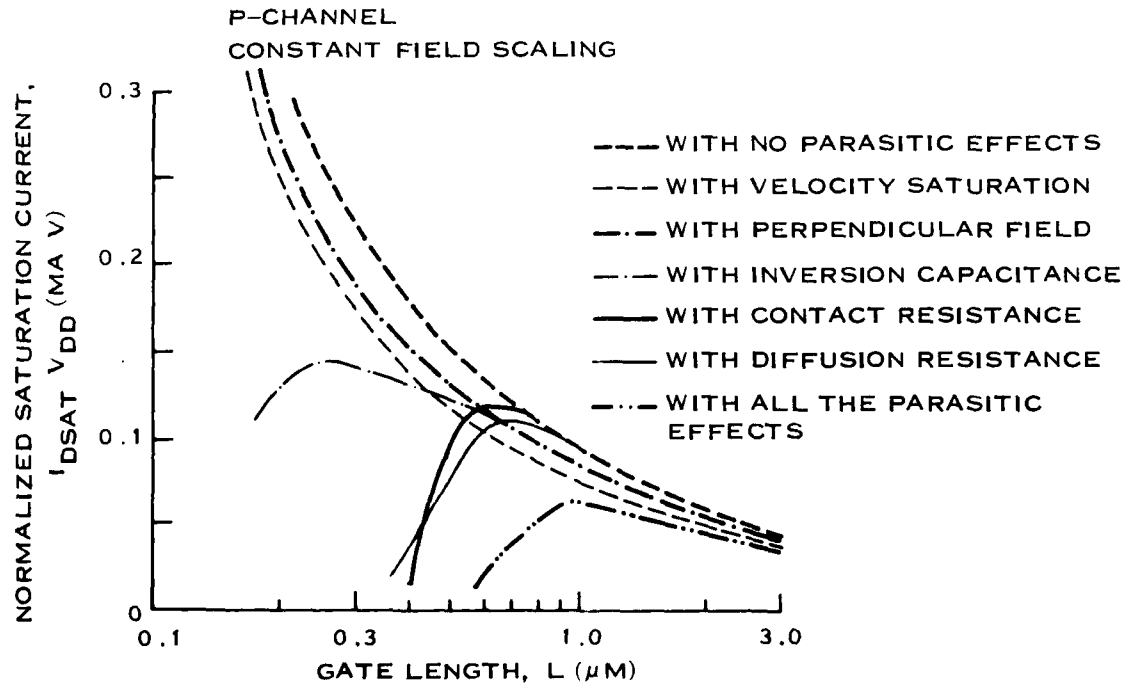
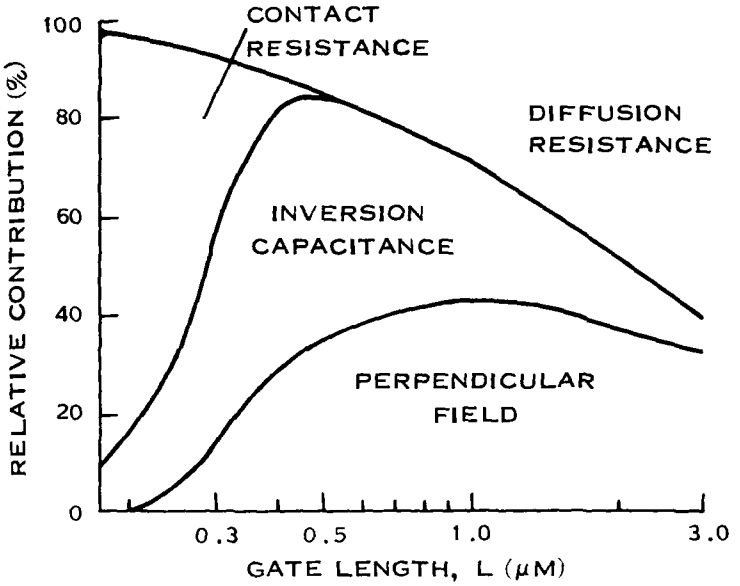
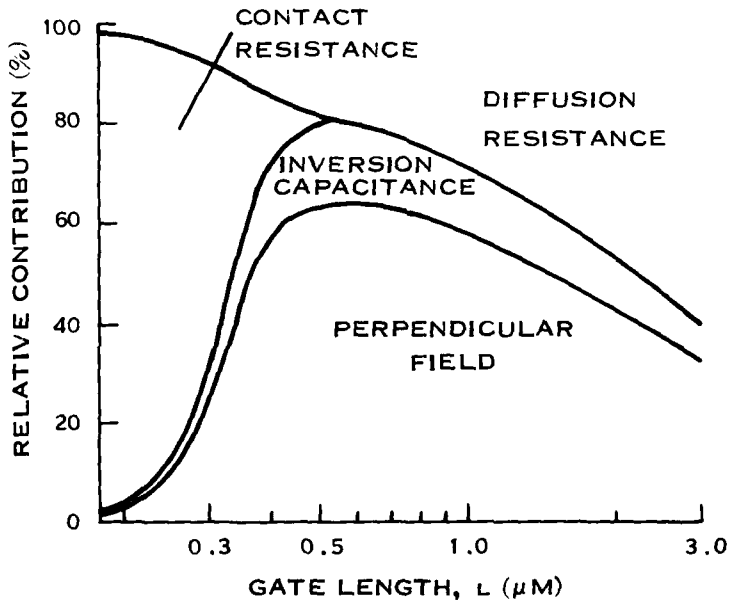


Figure 50. Variation of P-Channel Normalized Saturation Current Versus Gate Length With Each Parasitic Effect Added Separately



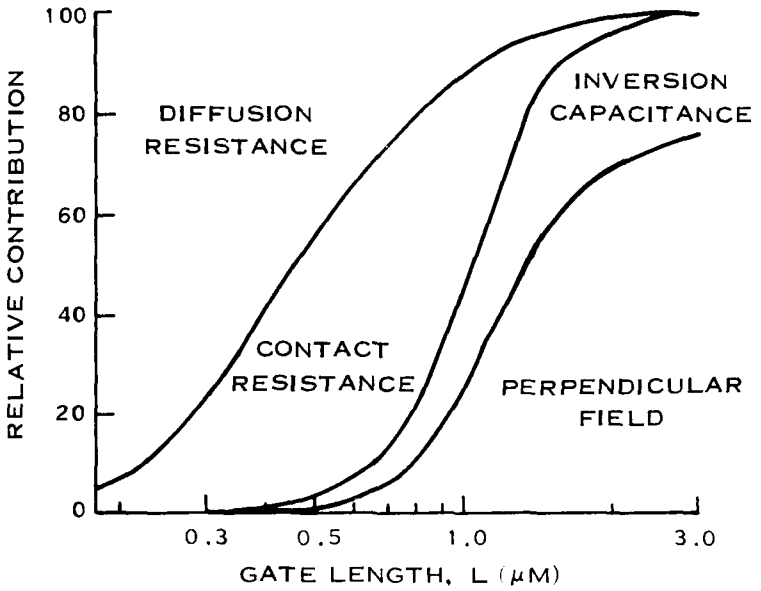
(A) CONSTANT FIELD SCALING

TRIODE GAIN N-CHANNEL



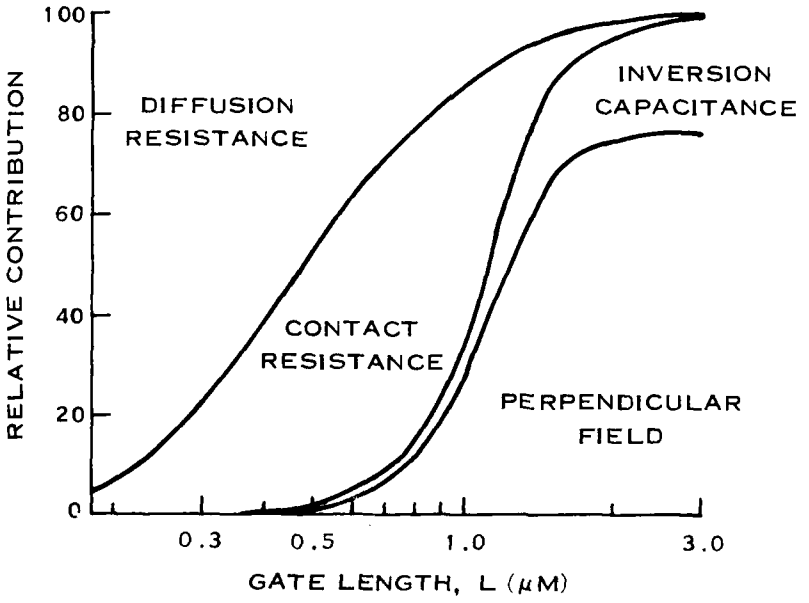
(B) CONSTANT VOLTAGE SCALING

Figure 51. Relative Contribution of Parasitic Effects to Gain degradation of N-Channel Devices



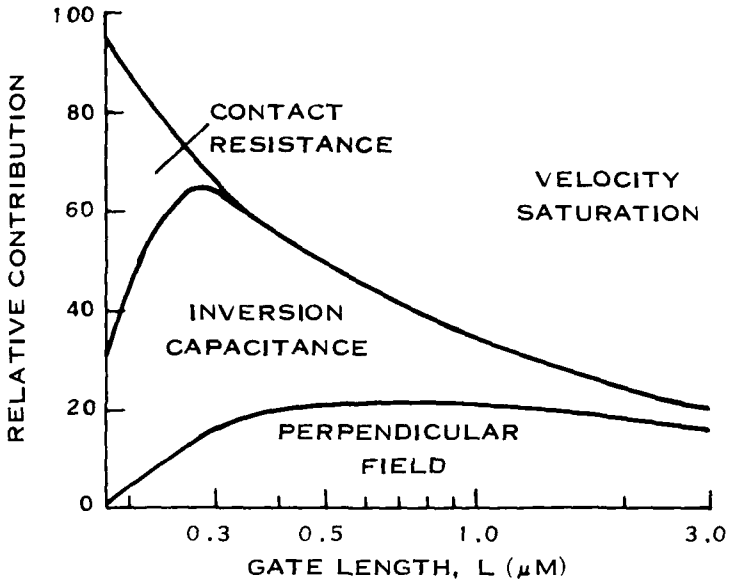
(A) CONSTANT FIELD SCALING

TRIODE GAIN P–CHANNEL



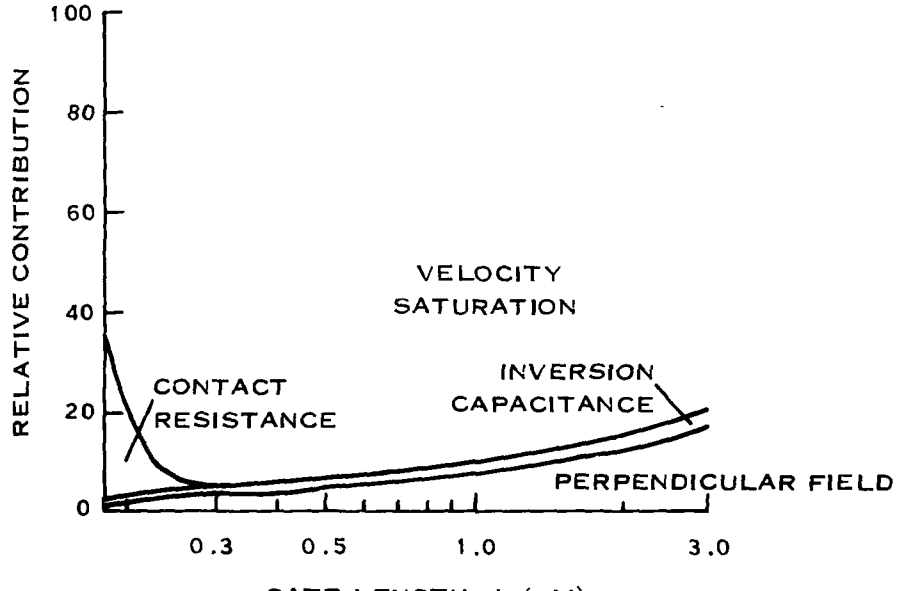
(B) CONSTANT VOLTAGE SCALING

Figure 52. Relative Contribution of Parasitic Effects to Gain degradation of P-Channel Devices



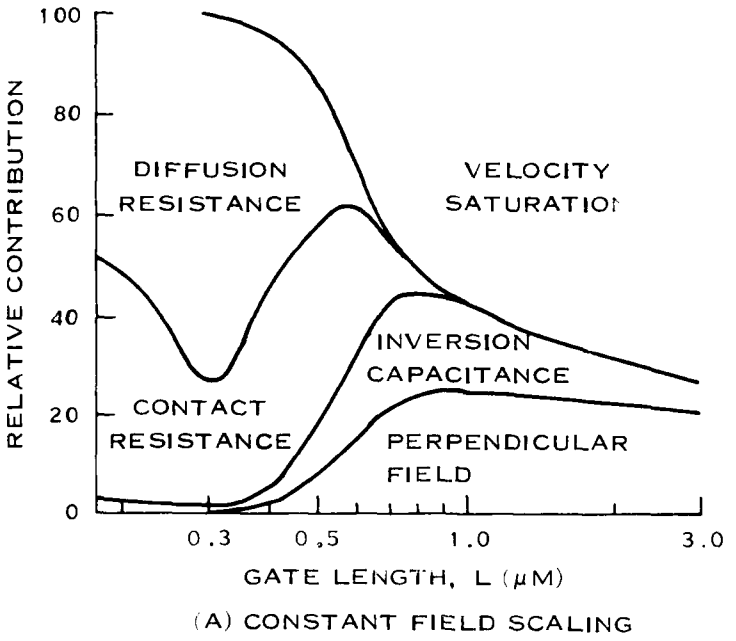
(A) CONSTANT FIELD SCALING

N-CHANNEL

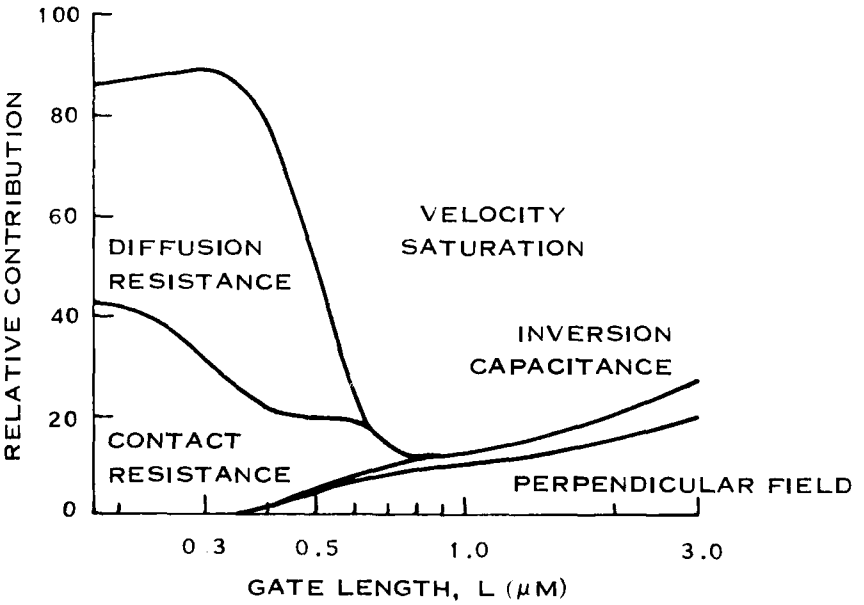


(B) CONSTANT VOLTAGE SCALING

Figure 53. Relative Contribution of Parasitic Effects to Saturation Current Degradation of N-Channel Devices



(A) CONSTANT FIELD SCALING



(B) CONSTANT VOLTAGE SCALING

Figure 54. Relative Contribution of Parasitic Effects to Saturation Current Degradation of P-Channel Devices

the opposite type, which reduces the electric field at the interface as described by Sun, et al.[64] Also shown in Figures 51 and 52 are the increasing contribution of contact resistance in both cases and diffusion resistance in the p-channel devices. Figures 53 and 54 show the large contribution of velocity saturation in degradation of the drain saturation current. This is particularly the case for n-channel devices because of the lower critical electric field.

2. Junction Depth

It should be clear from Figure 42 that the large increase in the parasitic source/drain series resistance for p-channel devices is caused by the linear scaling of the junction depth, x_j, that we have purposely imposed to illustrate the inadequacy of straightforward scaling. This causes a rapid increase in sheet resistivity. It also results in an increasing specific contact resistivity because of the decrease in the surface doping concentration as has been illustrated in Figure 43. In reality, this can be avoided by scaling the junction depth more gradually than the other dimensions, or even by keeping it constant at minimum tolerable depth ($\sim$0.4 μm). For example, shown in Figure 43 by a broken line is the case where the junction depth is scaled as $\kappa^{1/2}$ instead of linearly (κ). In this case, the gain peak for p-channel is expected to shift down to gate length of $\sim$0.4 μm.

However, this nonscaling of the junction depth results in an increasing short-channel effect and punchthrough. A simple estimate of the degree of short-channel effects can be obtained by the charge-sharing factor.[4] Figure 55 shows this sharing factor as a function of gate length under constant field scaling. The other scaling schemes give very similar results. When the junction depth is scaled linearly with the scaling factor κ, the charge-sharing factor remains around 0.8 so that short-channel effect is minimized. This has been assured by our scaling condition in Subsection II.B. When the junction depth is scaled as $\kappa^{1/2}$, however, a severe short-channel effect is expected below 0.6 μm. Keeping x_j constant at 0.4 μm worsens the situation, and the sharing factor drops below 0.5 at a gate length of $\sim$0.9 μm. Therefore, some compromise is necessary between the series resistance consideration and short-channel effects.

3. Critical Length, L_c

The importance of the critical length given by Equation (139) has been pointed out with regard to Figure 44. When a silicide region becomes shorter than L_c, the contact resistance becomes area-dependent[40] and increases sharply as the dimension is reduced further. Therefore, L_c sets a lower limit to the length of the source/drain region. For n-channel devices, this limit is $\sim$0.4 μm as shown in Figure 44. This is a practical limit on gate-to-contact separation in layout design of silicided MOS devices if silicided source/drains are to be beneficial in reducing series resistance.

G. CONCLUSIONS

A practical scalability limit of n- and p-channel devices has been reexamined including "higher order" effects, such as parasitic source/drain series resistance, mobility degradation from high electric fields, and inversion layer capacitance. It has been shown that even in constant field scaling, the channel doping must be increased more rapidly than $1/\kappa$, where κ is a scaling factor ($\kappa < 1$), because of the built-in potential. A recently developed transmission line model[40] was used to analyze the series resistance of the silicided source/drain region. This series resistance is shown to severely limit the device performance if the junction depth is scaled linearly with other dimensions. The triode gain peaks at a gate length of 0.4 μm for n-channel devices, and 1.4 μm for p-channel devices. From the degradation factor of triode gain and drain saturation current, a relative contribution of each parasitic effect on device performance has been examined.

[64]E. Sun, B. Heofflinger, J. Moll, and C. Sodini, "The Junction MOS (JMOS) Transistor—A High-Speed Transistor for VLSI," *IEDM Tech. Digest* (1980) pp. 791–794.

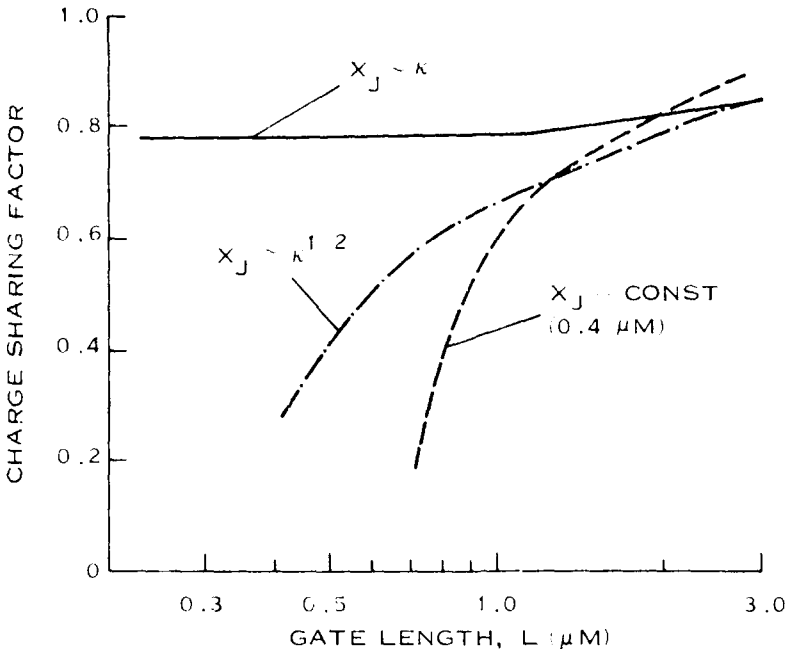


Figure 55. Variation of Charge-Sharing Factor Versus Gate Length for Three Different Scalings of Junction Depth

Based on these calculations, some modifications to straightforward scaling are shown necessary. First of all, the junction depth must be scaled more gradually than other dimensions with a risk of short-channel effect and punchthrough. This is particularly the case for p-channel devices because of the higher series resistance. The high series resistance is caused by both the increasing sheet resistivity and the increasing contact resistivity because of decrease in the surface doping concentration. Another important consideration in scaling is the concept of critical length, L_c. This length is shown to set a limit on the minimum separation between the gate and the contact to preserve the benefit of low-resistivity silicided source drain, which is of the order of 3 to 5 times the gate length.

Finally, the device performance of discrete devices is one of a number of factors that determine the actual scaling scheme in MOS technology. This paper has focused only on the device performance as affected by scaling. For example, by scaling the device beyond the peak of device performance, one can still obtain higher circuit density. A more comprehensive analysis is necessary to assess the overall performance/density/cost impact of different scaling schemes; it is beyond the scope of the present contract.

SECTION VI

LOW TEMPERATURE MEASUREMENTS

As channel lengths approach the mean free path of the electrons, the electron velocity can be greater than its equilibrium velocity as was first pointed out by Ruch.[45] Experimental observation of this ballistic transport effect has been complicated by difficulties of interpretation.[46] We have examined $L = 0.35\ \mu m$ MOSFETs produced by vertical etch technique[46] between 18° and 300°K with no evidence of ballistic transport.

An interesting phenomenon was observed in some of the devices caused by either an underlap of the source/drain region with the polygate or the thicker gate oxide near the source/drain as shown in Figure 56. The I-V characteristics of one of the devices are shown for T = 300°K in Figure 57 and T = 200°K in Figure 58. At 300°K, the parasitic series transistors, associated with the thicker gate oxide, control the device characteristics while, at lower temperatures, the mean free path of the electrons becomes long enough that an avalanche can occur at the chain of thick field devices. This results in a step function similar to an increase in drain current with V_{DS} where the higher current level is controlled by the thin-gate oxide transistor.

[45]J.G. Ruch, "Electron Dynamics in Short-Channel Field-Effect Transistors," *IEEE Trans. Electron Devices*, **ED-19** (1972), p. 652.

[46]J.J. Rosenberg, E.J. Yoffa, and M.I. Nathan, "Importance of Boundary Conditions to Conduction in Short Samples," *IEEE Trans. Electron Devices*, **ED-28** (1981), p. 941.

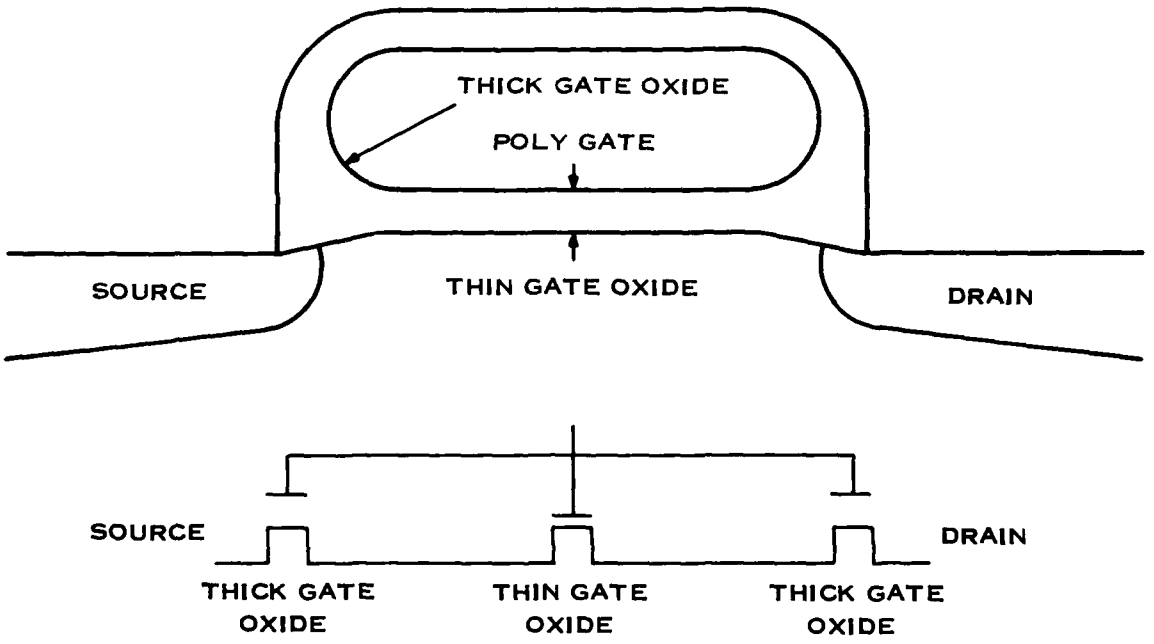


Figure 56. Vertical Etch Transistor Structure and Schematic of Parasitic Thick Gate Oxide Transistors

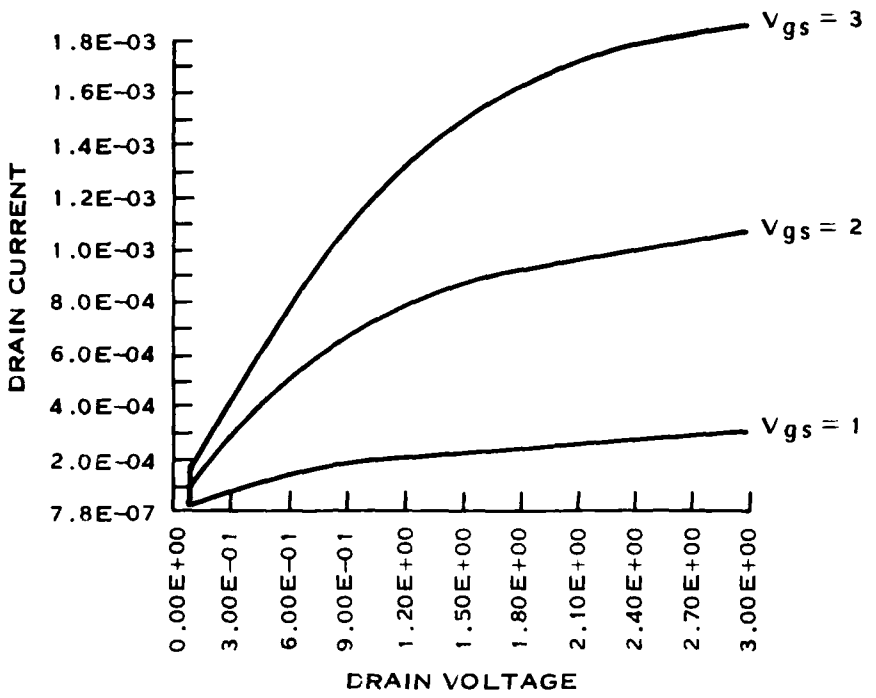


Figure 57. Vertical Etch Transistor (L = 0.35 μm) I-V Characteristics for T = 300 K

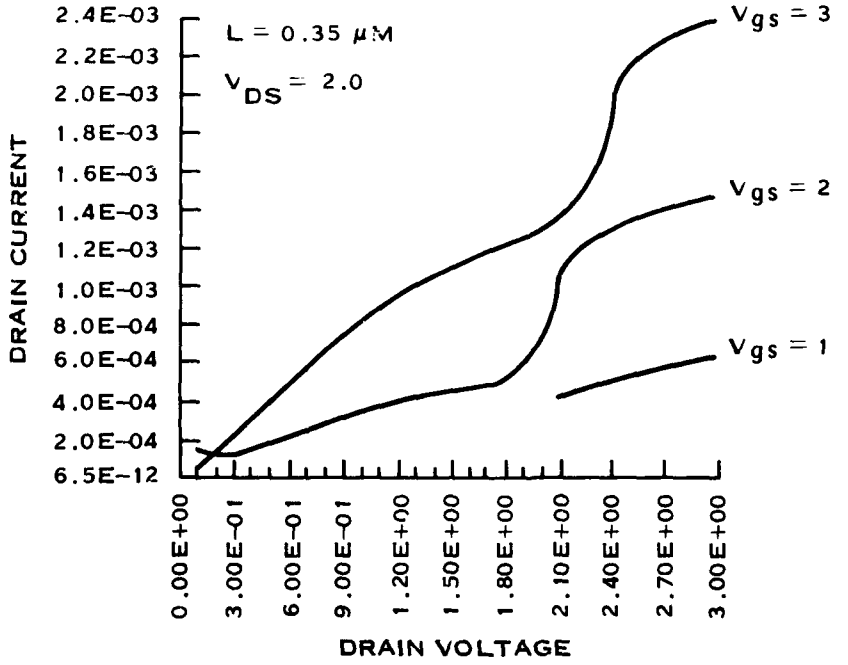


Figure 58. Vertical Etch Transistor I-V Characteristics for T = 200 K, Showing Avalanche Effects of Thick Gate Oxide Parasitic

SECTION VII

DRAIN-INDUCED SECONDARY IONIZATION EFFECTS IN SHORT-CHANNEL MOSFETs

At small geometry, MOSFETs biased in saturation have large electric fields near the drain region. The channel electrons gain sufficient kinetic energy in this drain field to generate electron-hole pairs by impact ionization. The electrons are mostly collected by the drain, and some hot elctrons are emitted over the SiO_2 barrier and may be trapped in the oxide to produce long-term reliability problems.[52] The holes are accelerated across the drain depletion region to form a substrate current as shown in Figure 59.

The substrate current is plotted as a function of gate voltage (Figure 60) for various drain voltages, for a 7.6-μm (0.3-mil) long, 127-μm (5-mil) wide device with 500-nm gate oxide. The substrate current for this long device can reach 1 μA for $V_{DD} \leq 10$ V. Thus, for a large circuit with many thousands of devices, the substrate current may easily be $\sim$1 mA (dc). This would cause significant debiasing for high resistivity substrates and make the design of on-chip substrate bias generators very difficult.

The second consequence of this hole current is even more serious. As the holes are accelerated out of the drain depletion region, they may gain enough kinetic energy to generate a secondary electron-hole pair by impact ionization. Most of the electrons are pulled into the drain, but those at the edge of the depletion region have enough energy to escape the drain field and diffuse into the substrate. This minority diffusion current is a strong leakage source because diffusion lengths are $\sim$400 to 600 μm in dynamic NMOS material.

To measure this effect, we have used a 150-bit shift register 368 μm (14.5 mils) from a set of MOSFETs as shown in Figure 61.[53] The MOSFET ($L = 7.6$ μm, $W' = 127$ μm, $t_{ox} = 500$ nm) is dc-biased in saturation; the CCD is cleared of charge and allowed to integrate charge for $\sim$1.5 seconds, after which the contents of the CCD wells are read out. Figure 62 shows the superposition of the collected charge in the CCD for three cases. The first, with no MOSFETs on, shows the residual leakage in the CCD. The

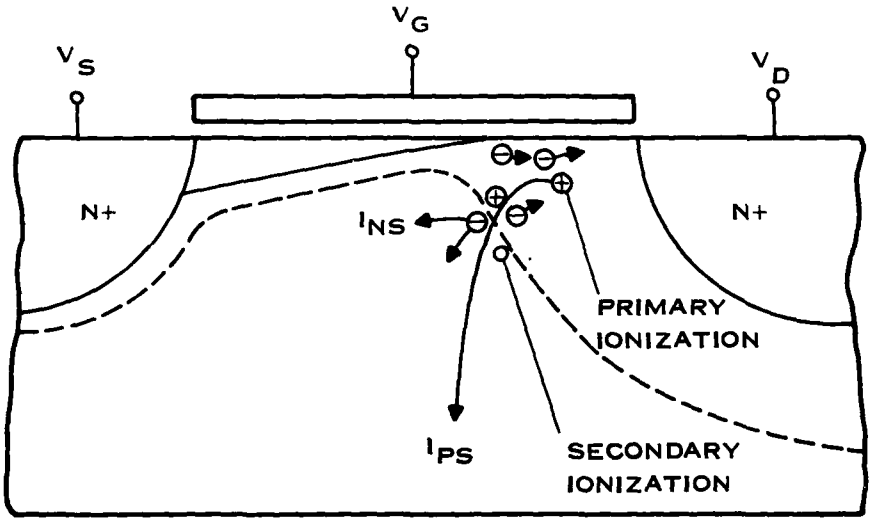


Figure 59. Primary and Secondary Impact Ionization in a Saturated MOSFET

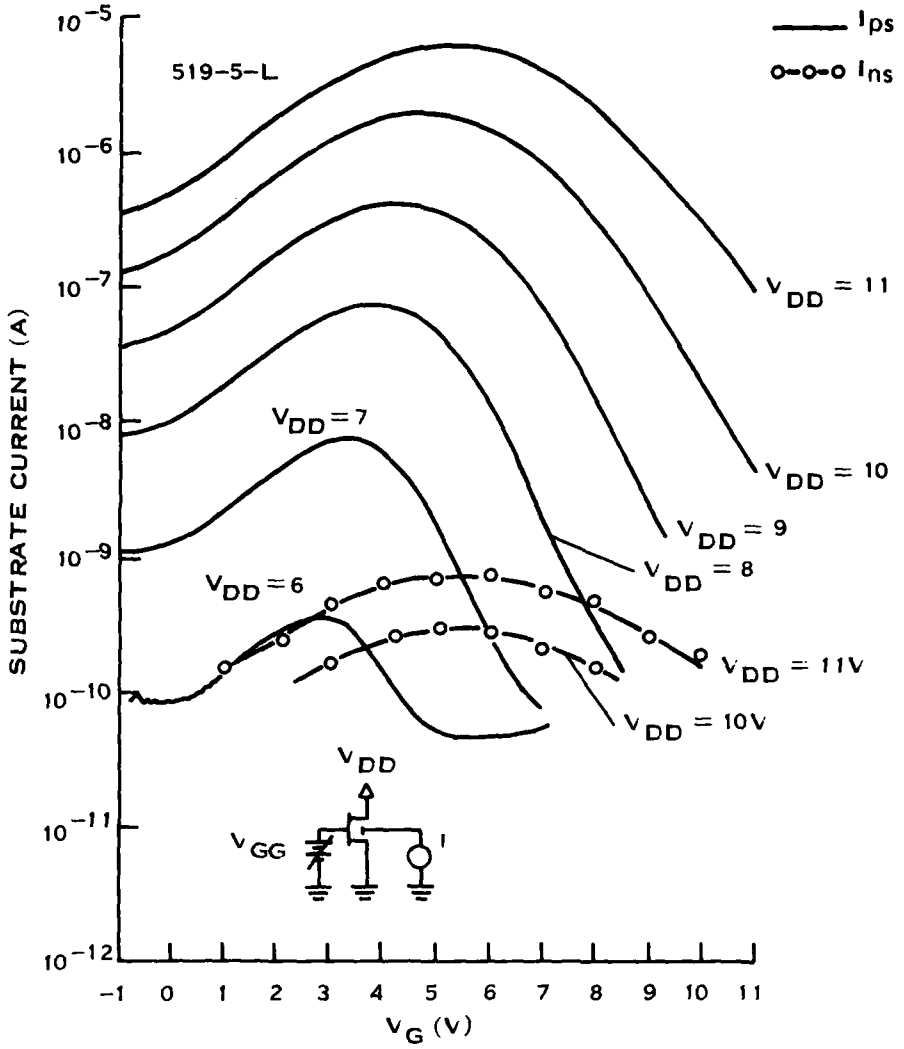


Figure 60. Substrate Hole Current and Secondary Impact Ionization Current Versus Gate Voltage

second and third have two different MOSFETs (2 and 7 in Figure 61) biased in saturation. The exponential decay of charge collected along the CCD provides a measure of the diffusion length of the minority carriers. The peak corresponds to the position of the MOSFET with respect to the CCD. The diffusion length as measured from Figure 62 is $L_n = 460\ \mu m$.

The current ΔI_p flowing into the pth CCD pixel dA of the CCD storage element is written as

$$\Delta I_p = \frac{I_{ns}\, e^{-x_p/L_n}\, dA}{(2\pi\, x_p^2)} \tag{145}$$

where x_p is the distance of the pth CCD pixel from the MOSFET, and I_{ns} is the secondary impact ionization-generated electron current. This diffusion is isotropic for a hemispherical shell of radius x_p, and the total current I_{ns} may be written as

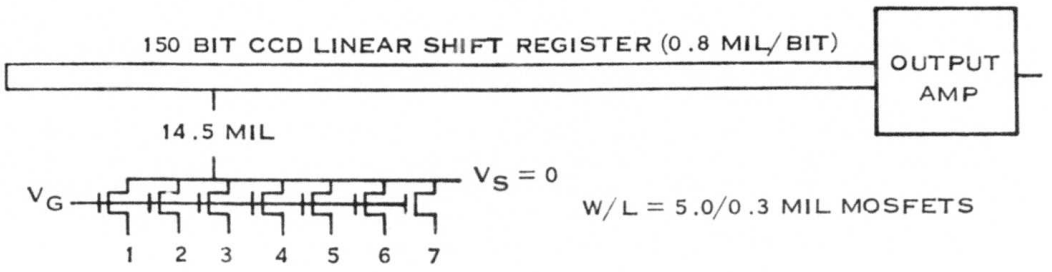


Figure 61. CCD Charge Detector Setup

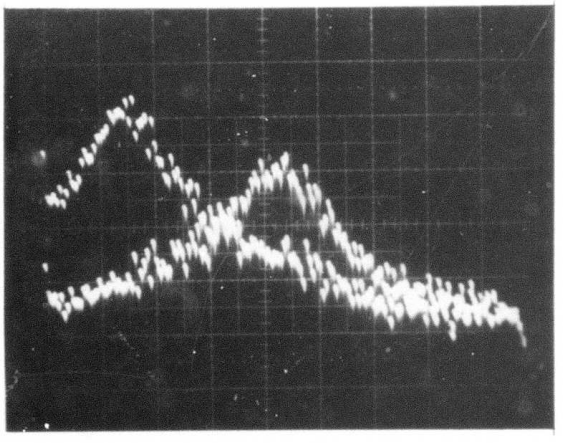


Figure 62. Secondary Electron Current From MOSFETs 2 and 7 Measured by CCD Charge Integration at Room Temperature

$$I_{ns} = \frac{2\pi x_p^2 \Delta I_p (e^{x_p/L_n})}{dA} \tag{146}$$

Figure 60 also shows the current I_{ns} as a function of V_G for $V_{DD} = 10$ and 11 V. From Figure 60, the probability of secondary electron emission to hole emission is $\sim 10^{-4}$.

Thus, each saturated transistor generates a leakage current source of $\sim 10\ \mu A/cm^2$ at room temperature compared with the more commonly observed generation rates of ~ 1 to 10 nA/cm^2. The long diffusion length makes this an extremely difficult design problem for dynamic NMOS circuits, which may have thousands of such sources in the periphery, and for memories where this could adversely affect the refresh requirements. This is difficult to model because it is a nonlocal effect.

The simple one-dimensional model described by Troutman[67] has been compared with experimental data. This model is based on several assumptions:

Ionization of secondary holes is negligible compared with ionization of primary electrons.

The drain junction is a one-dimensional abrupt p-n junction.

Using these assumptions, the multiplication factor M is defined by:

$$M = \frac{I_D}{I_S} \tag{147}$$

and can be obtained from

$$1 - \frac{1}{M} = \int_0^W \alpha\, dx = \left(\frac{\epsilon}{q N_A}\right) \int_{E_o}^{E_M} \alpha\, dE \tag{148}$$

where α is the electron ionization rate, $0 \le x \le W$ is the region where ionization occurs, N_A is the channel acceptor concentration, E_o is the electric field at the pinch-off point, and E_M is the maximum electric field at the drain. The dependence of the ionization rate on the electric field can be expressed as[67,68]

$$\alpha\lambda = \exp\left[-a_0 - a_1 Z - a Z^2\right] \tag{149}$$

where

$$a_0 = 757r^2 - 75.5r + 1.92 \tag{150}$$

$$a_1 = -46r^2 + 11.9r - 1.75 \times 10^{-2} \tag{151}$$

$$a_2 = -11.5r^2 + 1.17r - 3.9 \times 10^{-4} \tag{152}$$

$$r = \frac{\phi_P}{\phi_I} \tag{153}$$

[67]R.R. Troutman, "Low-Level Avalanche Multiplication in IGFETs," *IEEE Trans. Electron Devices*, ED-23 (1976), pg. 419.

[68]C.R. Coswell and S.M. Sze, "Temperature Dependence of Avalanche Multiplication in Semiconductors," *Appl. Phy. Lett.*, 9 (1966), p. 242.

and

$$Z = \frac{\phi_I}{\lambda E} \tag{154}$$

In the above expressions, λ is the optical mean free path, ϕ_P is the Raman optical phonon energy, ϕ_I is the threshold energy for impact ionization, and E is the electric field. Integrating Equation (148) yields

$$1 - \frac{1}{M} \approx \left(\frac{\epsilon}{qN_A}\right)\left(\frac{\phi_I}{\lambda^2}\right)\frac{\lambda\, \alpha\, rZ_m}{Z^2 M\,(\lambda a_2 Z_m + a_1)} \tag{155}$$

where

$$Z_M = \frac{\phi_I}{2E_M}$$

For the saturation region, the peak electric field is given by

$$E_M = \sqrt{\frac{2qN_A}{\epsilon}\,(V_D - V_{DSAT})} \tag{156}$$

where V_{DSAT} is the saturation voltage calculated by the charge-sharing model. The substrate current is then given by

$$I_{sub} = (M - 1)\, I_s \tag{157}$$

where I_s is the source current.

In the devices we have fabricated, the source/drain region has an extension that is more lightly doped than the normal source/drain region. The purpose of this extension is to reduce the magnitude of the electric field at the drain end of the channel.[49] When evaluating Equation (155) to determine the maximum electric field, N_A must be replaced by

$$N_E = \frac{N_A\ \ N_D}{N_A + N_D} \tag{158}$$

where N_A is the channel concentration and N_D is the concentration of the lightly doped source/drain. This reduces the effective doping from 2.80×10^{16} cm^{-3} to 2.71×10^{16} cm^{-3}. The values of ϕ_P and ϕ_I used in the calculation are the room temperature values of

$$\phi_P = 0.053 \text{ eV and } \phi_I = 1.68 \text{ eV} \tag{159}$$

The calculated value overestimates the measured value of substrate current. This is expected because Equation (155) assumes an abrupt p-n junction. An adjustment for this assumption is made by scaling the maximum electric field calculated for Equation (155) by a constant factor so that the calculated and measured peak substrate currents are equal. This electric field reduction factor was found to be 1.26 for the devices under study.

The results of the calculations after adjustment of E_M are compared with the experimental measurements in Figure 63. E_M has been adjusted at the peak substrate current for $V_{DS} = 5$ V. Agreement between the model and the experiment is good except at low V_{DS}. Figure 64 shows the same results in terms of the

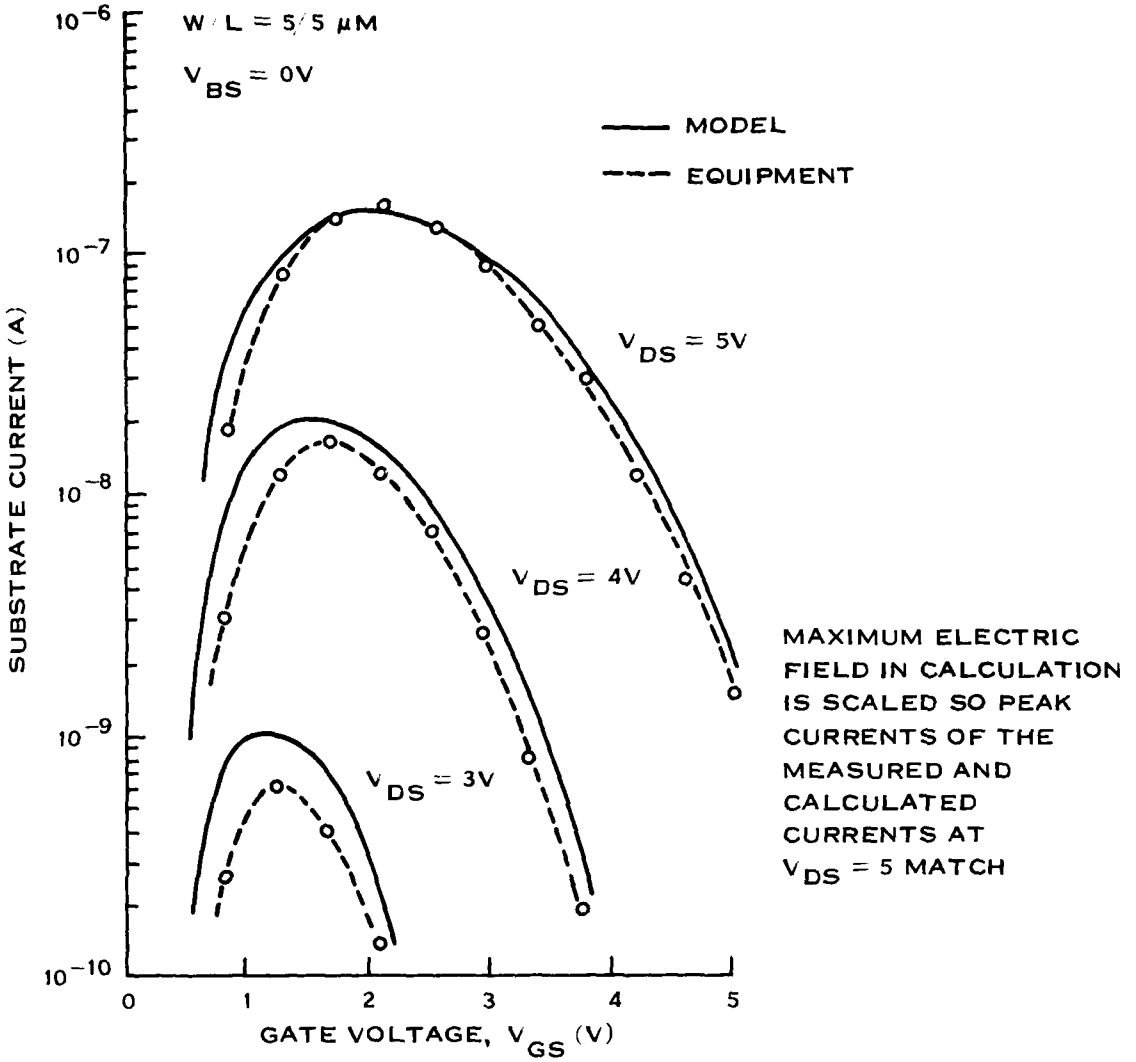


Figure 63. Comparison of Calculated and Measured Substrate Current

multiplication factor, $M - 1 = I_{sub} / I_s$. Again, the agreement is good. The better agreement at low V_{DS} suggests that the discrepancy in Figure 63 is caused by the difference in channel current, not in the multiplication factor.

Figures 65 and 66 compare the calculated and measured values for a channel length of 1 μm. The calculated values are obtained using the same parameters used for the 5-μm device shown in Figures 63 and 64. The model predicts the correct behavior of the multiplication factor as shown in Figure 66 and qualitatively agrees with the experimentally obtained substrate current shown in Figure 65.

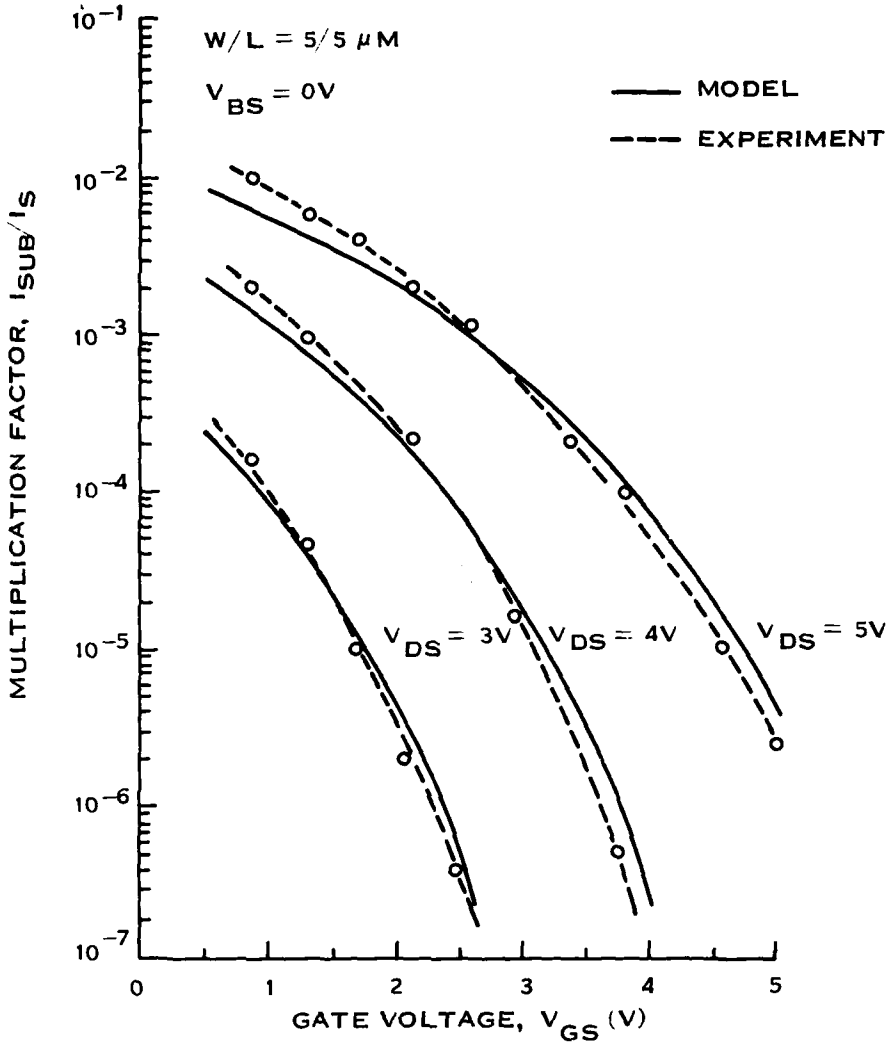


Figure 64. Comparison of Calculated and Measured Multiplication Factor Corresponding to Figure 63

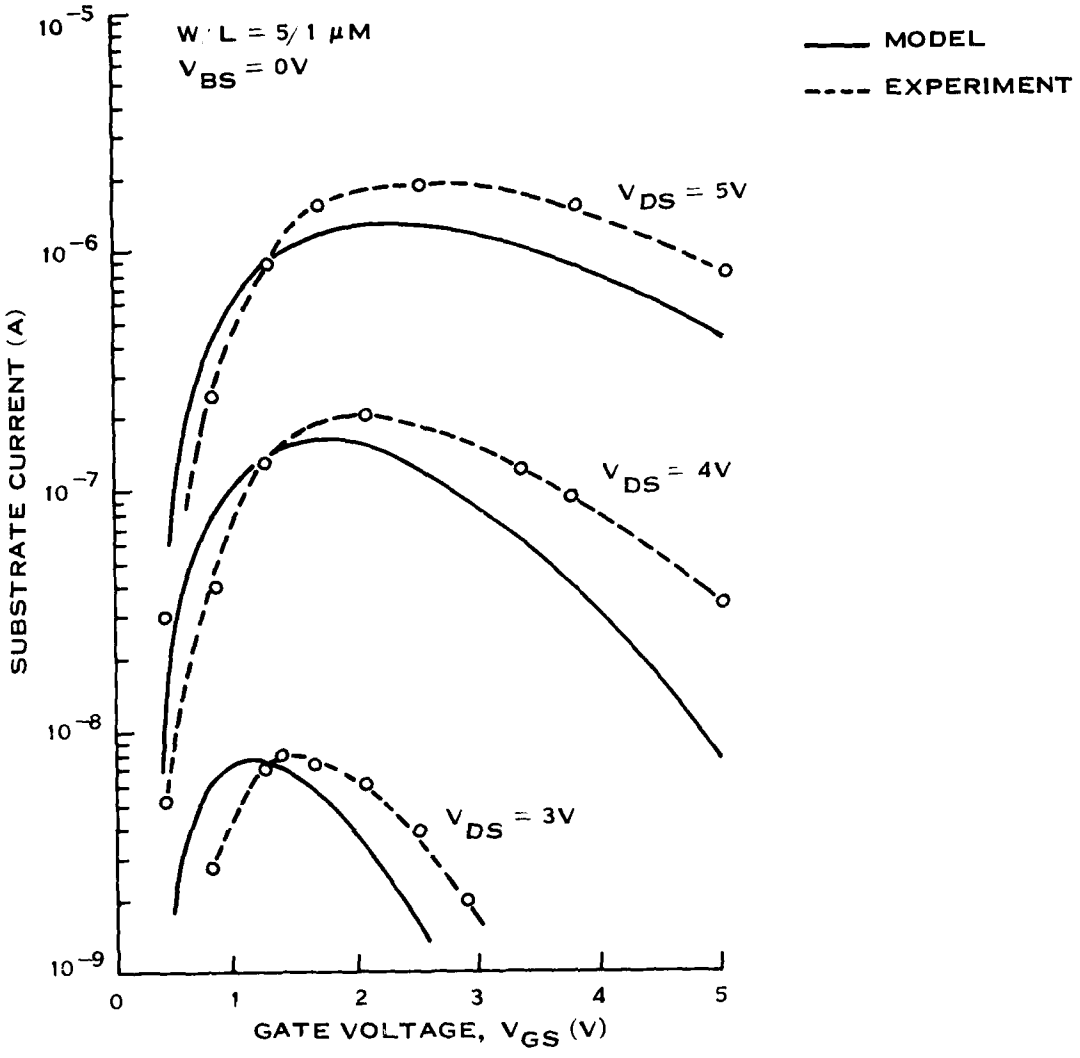


Figure 65. Comparison of Calculated and Measured Substrate Current for Shorter Channel Length Device

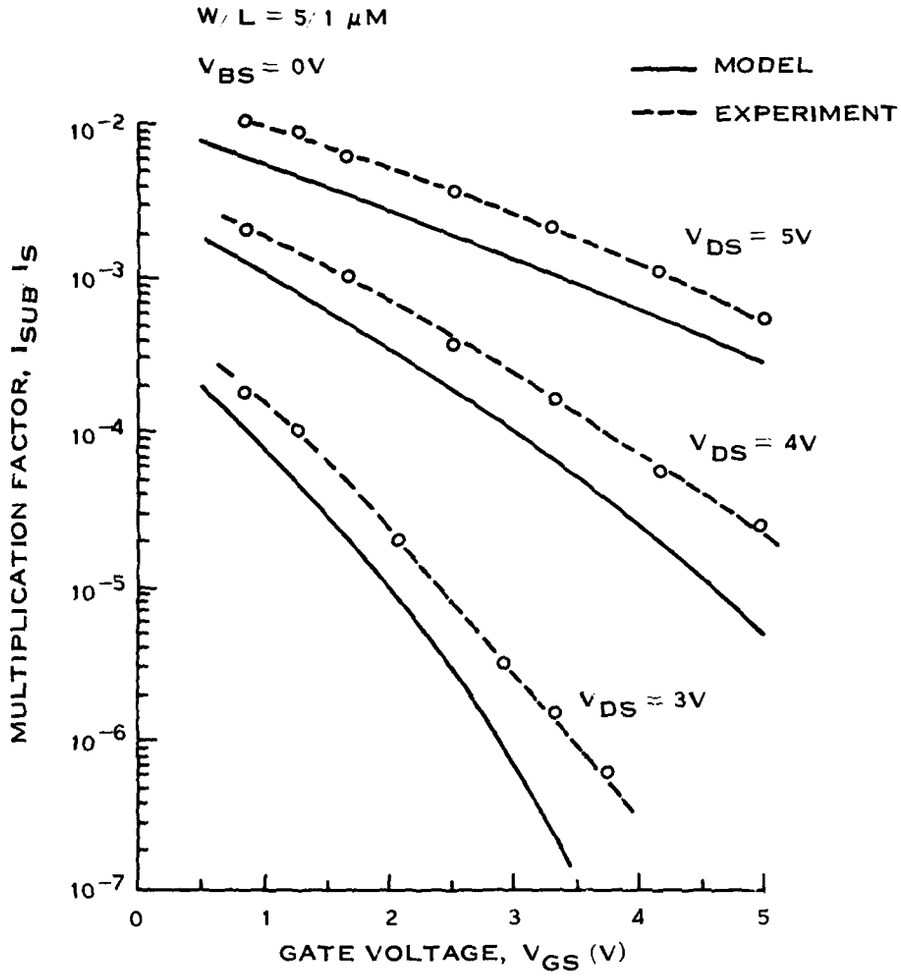


Figure 66. Comparison of Calculated and Measured Multiplication Factor Corresponding to Figure 64

SECTION VIII

MEASUREMENT OF MOSFET CAPACITANCES

A. MEASUREMENT OF C_{gs} and C_{gd}

Accurate measurement of the incremental capacitances, especially C_{gd}, is extremely difficult because of the biasing requirements. We have attempted this measurement using the approach discussed below.

A Boonton Model 75C Direct Capacitance Bridge was modified for the measurements. To better understand the problems associated with this measurement and the necessity for the modifications, consider the schematic representation in Figure 67(a), which shows the bridge circuit with the MOSFET being measured represented by two capacitors and a channel resistor. This is the configuration for measuring C_{gd}. The source is grounded to eliminate C_{gs} and the channel resistor from the measurement. However, grounding the source dc-shorts it to the drain through the transformer windings. To apply V_{DS}, it is necessary to add a capacitor to dc-isolate the center tap of the transformer from ground. V_{DS} V_{GS} can then be applied through the detector lines and chassis ground.

Another problem arises from attempting to make the device large enough for intrinsic capacitances to dominate the measurement. The channel resistance can thus be very small. This small channel resistance appears across one side of the transformer. In an inductive ratio bridge,[51] the inductors are wound on the same core so that at null the mutual inductance exactly cancels the magnetic flux from self inductance; thus, the only impedance is that of the resistance of the transformer windings, which can be on the order of the channel resistance. To keep the bridge symmetrical, another resistor with the same value as the channel resistance must be placed across the other transformer arm. If there is no gate resistance, it should be possible to measure the capacitances independently. If the gate resistance is not neglected, the modified bridge circuit with MOSFET can be schematically represented as shown in Figure 67(b).

The large area enhancement MOSFETs on the e-beam lot have polysilicon gates. The resistance of these gates is too large to allow capacitance measurements even at the reduced frequencies afforded by the use of the lock-in amplilfier.

While C_{gs} no longer appears directly across the detector, it is included in the measurement along with the gate resistance, r_{gg}'. The measured value of the unknown will be frequency-dependent within the normal frequency range of the bridge. Circuit analysis of this bridge configuration with the gate resistance and capacitance replaced with a transmission line is very difficult. A possible solution pursued in this problem is to eliminate the internal detector and frequency source and replace them with external parts capable of lower frequencies, less than 5 kHz. As the frequency is lowered, the impedance of the gate resistance becomes less than the impedance of the gate capacitances, and the measured value should asymptotically approach the desired unknown capacitance.

The internal frequency source and detector of the Boonton 75C Direct Capacitance Bridge was replaced by a PAR Model 126 Lock-In Amplifier with a Model 184 Current-Sensitive Preamplifier and a Model 127 Two-Phase Accessory, allowing low-frequency capacitance measurements. C_{gd} measurements were made as functions of V_{GS} and V_{DS} as shown in Figure 68. The C_{gd} measurement is relatively insensitive to the substrate bias as shown in Figure 69.

This capacitance measurement technique is capable of distinguishing between nonreciprocal capacitances. The capacitances C_{bg} and C_{gb} have been measured on a different device using the experimental setup shown in Figures 70 and 71. The results of C_{bg} measurements at several V_{BS} are shown in Figures 72 and 73 while C_{gb} measurements are shown in Figures 74 and 75. The values of C_{bg} and C_{gb} for $V_{BS} = 0$, shown in Figures 73 and 75, are replotted in Figure 76 showing that C_{bg} and C_{gb} are nonreciprocal in the

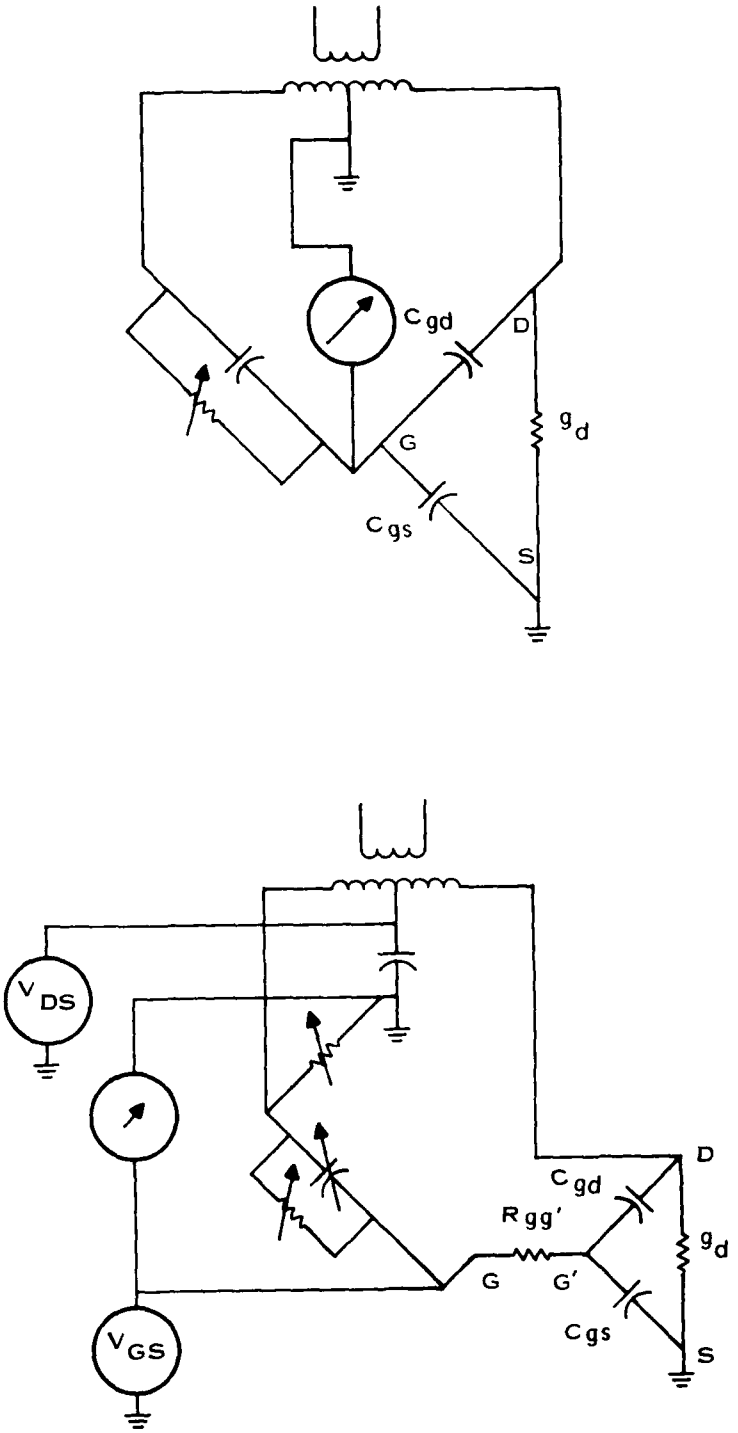


Figure 67. Schematics of Bridges to Measure MOSFET C_{gd}

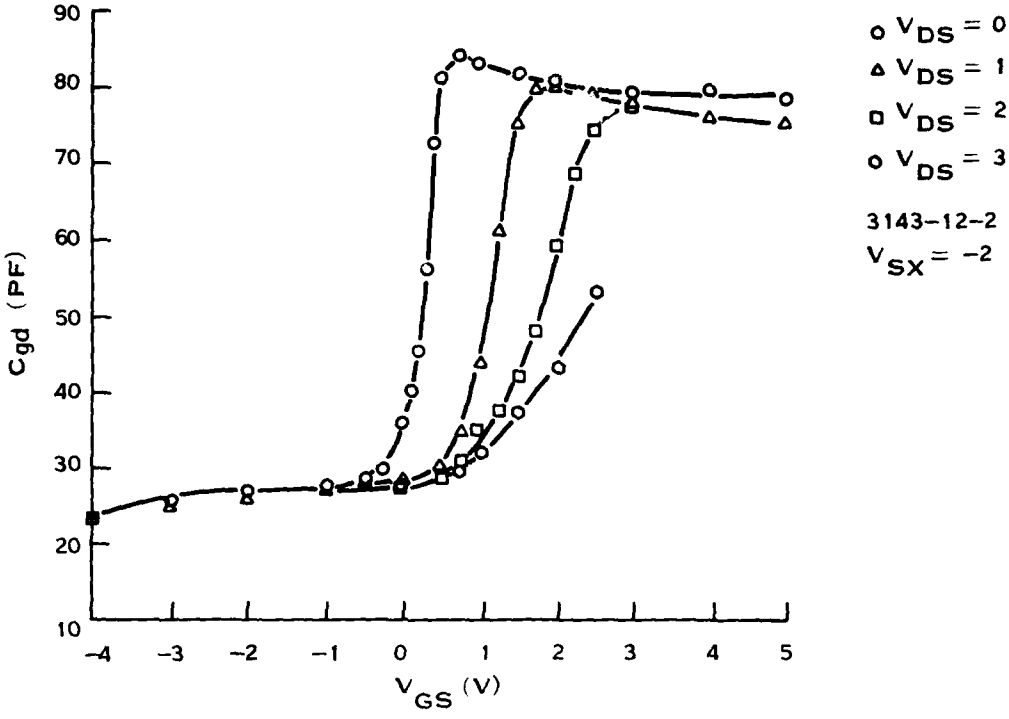


Figure 68. Measured Gate Voltage Dependence of C_{gd} Under Actual Bias Condition Versus V_{DS}

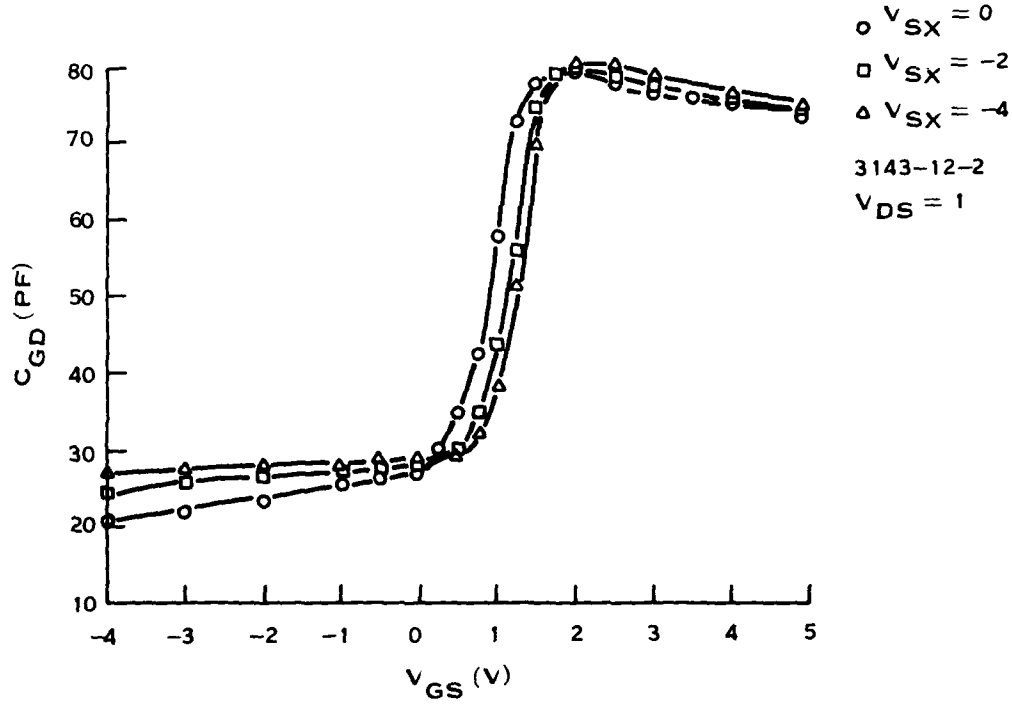


Figure 69. Measured Gate Voltage Dependence of C_{gs} Under Actual Bias Condition Versus Substrate Bias V_{sx}

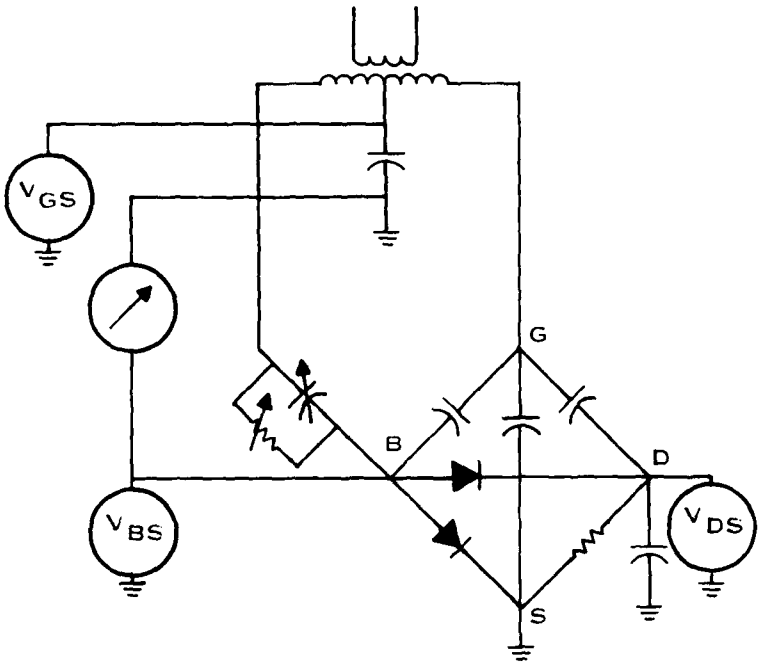


Figure 70. Configuration For Measuring $C_{bg} = 2Q_B/2\ V_G$

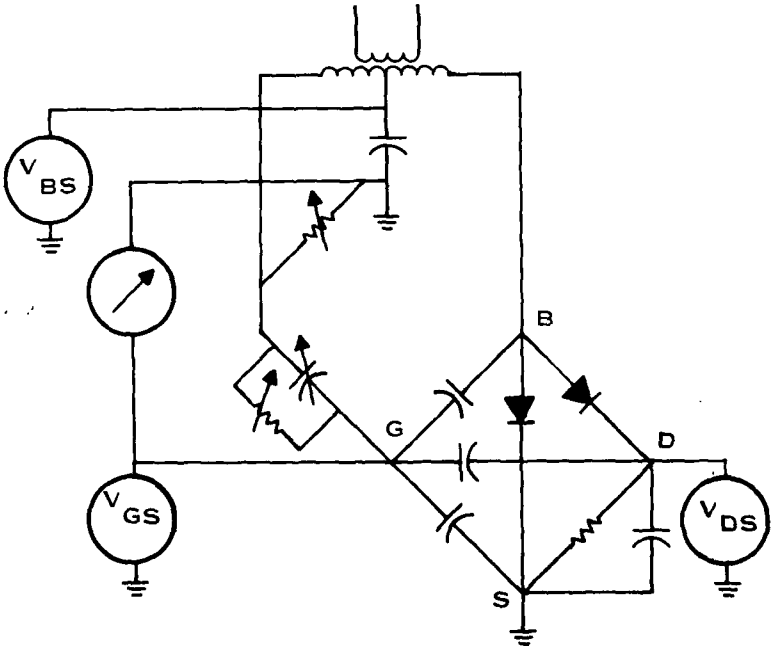


Figure 71. Configuration for Measuring $C_{gb} = 2Q_g/2\ V_B$

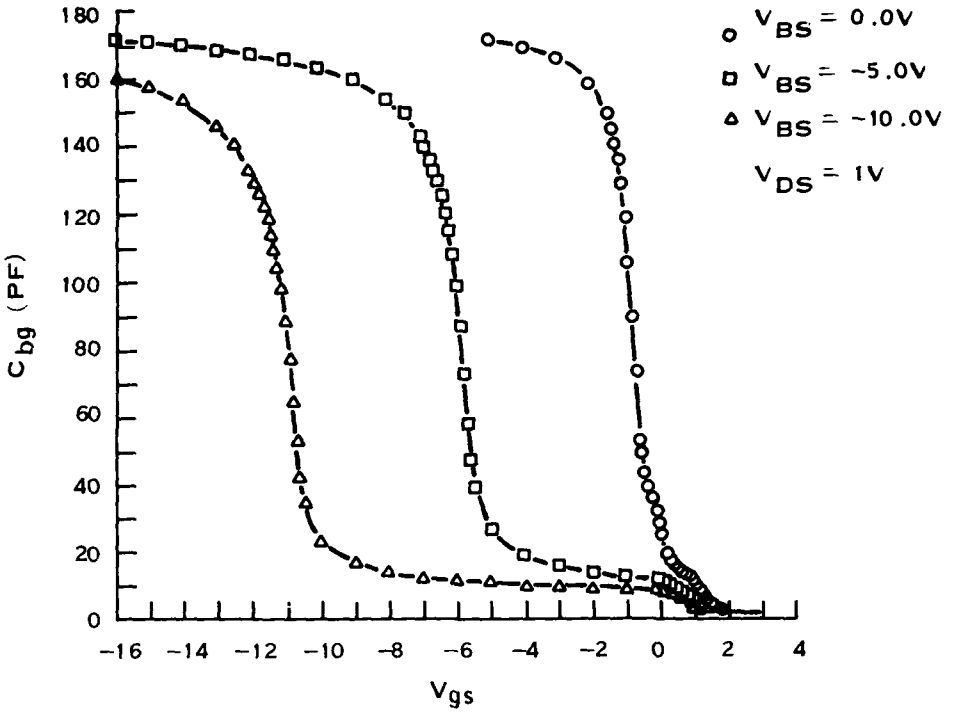


Figure 72. C_{bg} Versus V_{GS} for Three V_{BS} Values

saturation region. It is expected that the impact of this nonreciprocity will have negligible effect on circuit simulation results because in the saturation region the nonreciprocal component of C_{bg} and C_{gb} is only ~1 percent of the total oxide capacitance.

B. FRINGE CAPACITANCE C_{FR} CAUSED BY FINITE GATE ELECTRODE THICKNESS

For long channel MOSFETs, it is sufficient to use the parallel-plate equation to calculate the capacitance. The parallel-plate capacitance equation is accurate if the channel length and width are much greater than the thickness of the gate oxide and the gate electrode. The scaling down of MOSFETs has made the channel length, width, and the thickness of the gate electrode comparable, thus the fringe capacitance (C_{FR}) becomes as important as the oxide capacitance (C_{ox}) and must be added to the parallel-plate capacitance to obtain an accurate representation (Figure 77).

The fringe capacitance C_{FR} can be obtained by using conformal mapping and solving the Laplace equation. Define

$$x = \frac{t_{ox}}{t_{poly}}$$

then

$$C_{FR} = \frac{\epsilon_{ox}}{\pi}\left[\left(x + \frac{1}{x}\right)\ln\left(\frac{1+x}{1-x}\right) + 2\ln\left(\frac{1}{4}\left(\frac{1}{x} - x\right)\right)\right] \tag{160}$$

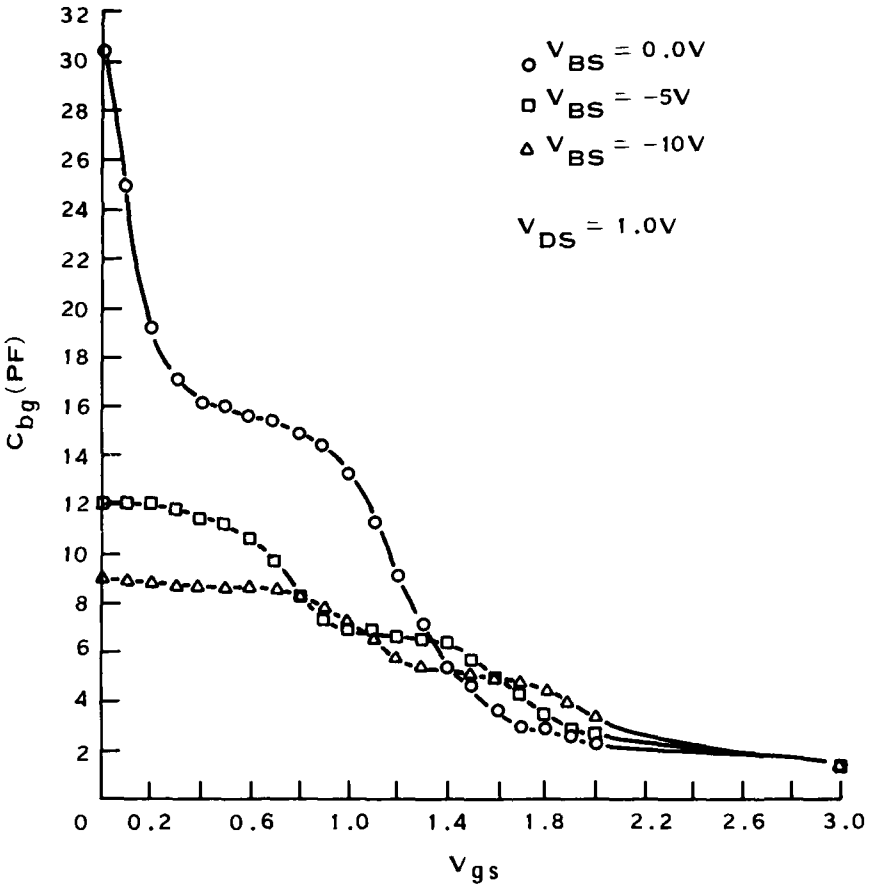


Figure 73. Detail of Nonreciprocal Portion of Figure 72

where

t_{ox} = the gate oxide thickness

t_{poly} = the gate electrode thickness.

As the device channel length is scaled down, the total oxide capacitance is reduced proportionally. If the gate electrode thickness is not scaled down or the gate oxide thickness is not scaled down, the fringe capacitance C_{FR} will become dominant. This can be seen from the plots of C_{FR}/C_{ox} given in Figure 78(a), (b), and (c). These plots also show that conventional scaling laws must be modified to include the effects of fringe capacitance.

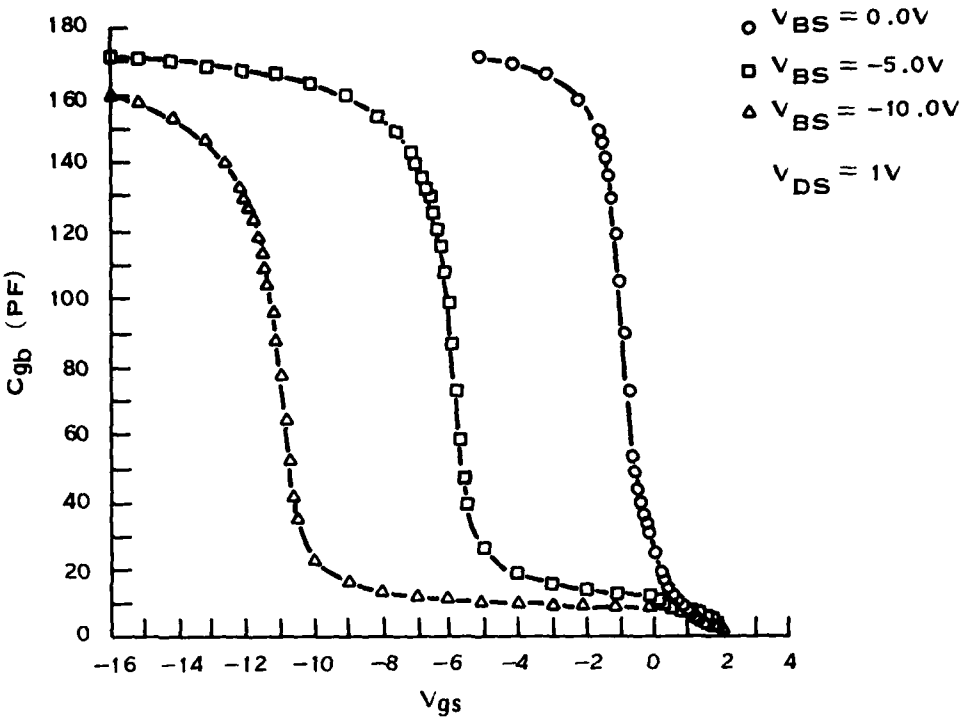


Figure 74. C_{bg} Versus V_{GS} for Three V_{BS} Values

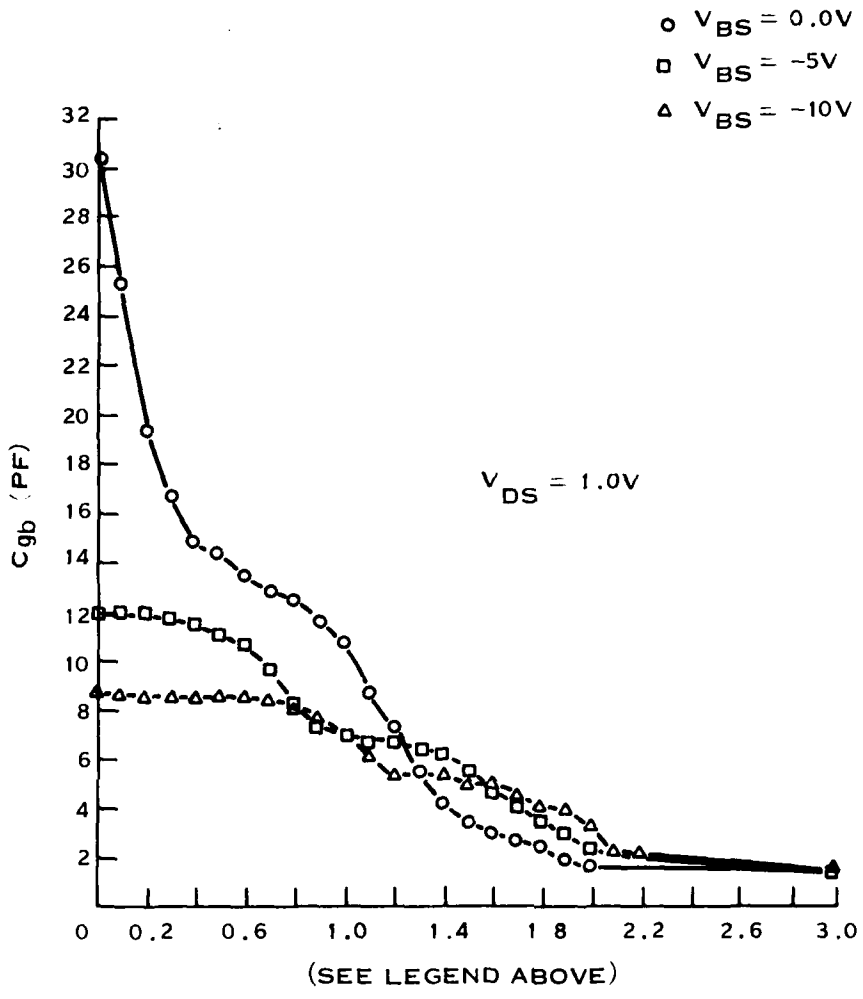


Figure 75. Detail of Nonreciprocal Portion of Figure 74

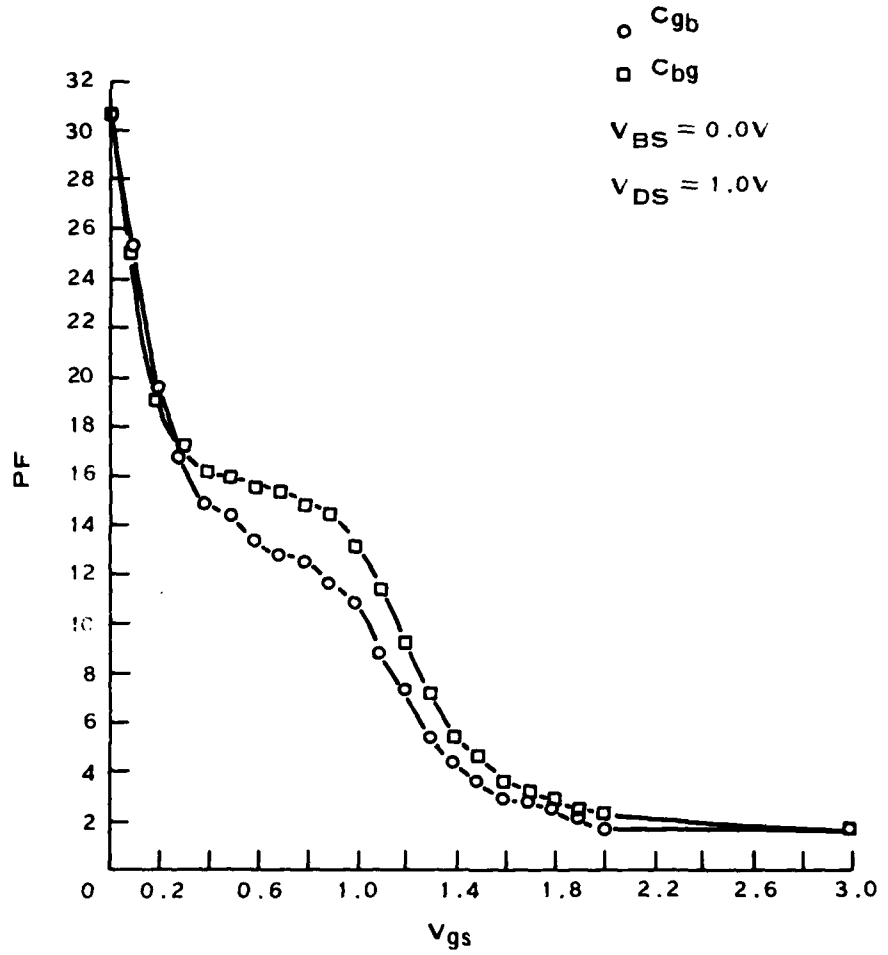


Figure 76. C_{bg} and C_{gb} Versus V_{GS} for V_{BS} = 0 Showing Nonreciprocal Nature of Gate to Bulk Capacitance

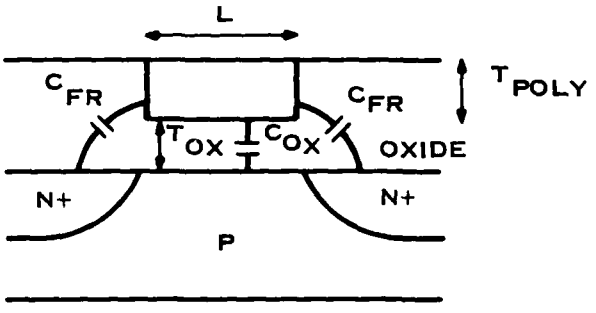
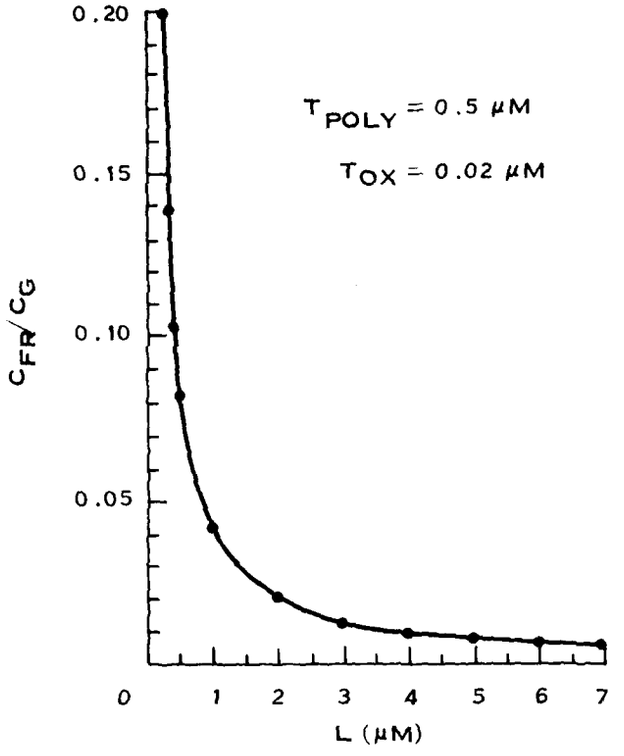


Figure 77. Fringe Capacitance of a MOSFET



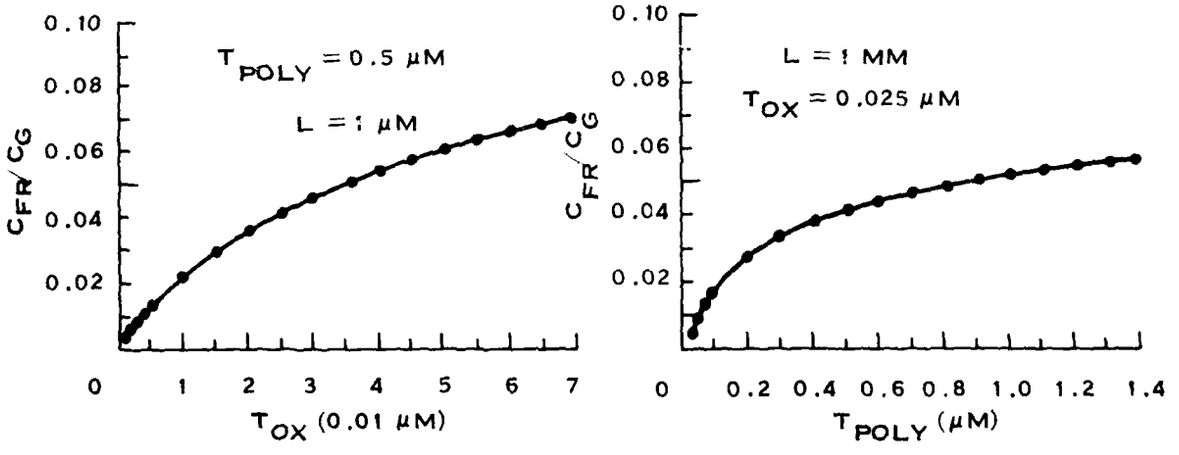


Figure 78. C_{FR}/C_G Versus Channel Length and Oxide Thickness

SECTION IX

COMPUTATIONALLY EFFICIENT SHORT-CHANNEL MOSFET CURRENT MODEL FOR VLSI CIRCUIT SIMULATION

The scaling down of MOS transistors for VLSI has created new demands for short-channel MOSFET models. Two-dimensional effects, high drain field effects, and soft turnoff characteristics must be included in short-channel MOSFET models for circuit simulators. However, VLSI circuit simulations require that 10,000 device circuits be analyzed so that the device model does not reduce computational efficiency. Although excellent numerical and detailed analytical models have been reported,[5,68,69-71] which can accurately represent the short-channel effects, none are sufficiently efficient for VLSI circuit simulation. For example, even the analytic charge-sharing developed under this contract has a speed disadvantage 30 times that of the modified Shichman-Hodges model used in SPICE2.[72] The only feasible models for a circuit simulator are the quasi-physical models with parameters that can be extracted from data. Subthreshold current models have not been implemented in circuit simulators previously. The main obstacles are the complicated equations and the abrupt transition from below to above threshold, obstacles that cause substantial execution time and convergence problems. A smooth transition of the current among different regions is a requirement for any VLSI circuit simulation model. This is also true for the charges as reported in Section IV.[73] An important point to be noted is that only currents and charges must be continuous while derivatives of currents and capacitances do not.[73]

A simple and efficient MOSFET current model, which can accurately represent the short-channel effects and is suitable for VLSI circuit simulation, is described. The threshold voltage model is based on the charge-sharing concept and, hence, can account for the short-channel effects and the drain-induced barrier lowering. The model equation is simplified for fast execution in a circuit simulator. The current model contains current components both below and above threshold. The transition from the subthreshold region to the region above is simple and smooth. Several articles have appeared in the literature that deal with subthreshold conduction.[5,69] The concept used is that the above-threshold current model contains only the drift component and that the absence of the diffusion component is the reason the conventional above-threshold current model does not contain the subthreshold component. Using this concept for the region below threshold, the diffusion current component is solved and this component becomes the subthreshold current. As the subthreshold current contains only the diffusion component, a current discontinuity exists at the transition point between the regions. A fudge factor must be introduced to resolve this discontinuity. It will be shown that the above concept is wrong. In fact, the conventional equations for current above threshold contain both drift and diffusion components. The actual reason the conventional above-threshold current equations do not contain a subthreshold component is the use of the strong inversion assumption. The strong inversion assumption results in zero mobile charge density in the subthreshold region, which in turn results in zero subthreshold current. The small but finite subthreshold mobile charge density can be obtained by solving the Poisson's equation with proper approximations. The actual mobile charge density can be approximated by adding this small subthreshold mobile charge density to the mobile charge density computed by the strong inversion assumption. Using this approach and the above simple threshold voltage equation, a unified short-channel MOSFET current model is obtained.

[69]J.R. Brews, "A Charge-Sheet Model of the MOSFET," *Solid-State Electronics* **21** (1978) p. 345.

[70]W. Fichtner, R.L. Johnston, and D.J. Rose, "Three-Dimensional Numerical Modeling of Small-Size MOSFETs," 39th Device Research Conference, Santa Barbara, California (1981).

[71]S. Selberhers, A. Sch(two accent marks over the next character)utz, and H.W. Potzl, "MINIMOS—A Two-Dimensional MOS Transistor Analyzer," *IEEE Trans. Electron Devices* **ED-27** (1980) p. 1540.

[72]L.W. Nagel, "SPICE2: A Computer Program to Simulate Semiconductor Circuits," ERL Memo No. ERL-M520, Electronics Research Laboratory, University of California at Berkeley (May 1975).

[73]P. Yang, B. Epler, and P.K. Chatterjee, "A Charge Conserving Capacitor Model for VLSI MOSFET Circuit Simulation," 39th Device Research Conference, Santa Barbara, California (1981).

[74]T. Furuyana, S. Saito, and S. Fujii, "A New Sense Amplifier Technique for VLSI Dynamic RAMs," *IEDM Technical Digest* (1981).

This current model contains components both above and below threshold. There is no current discontinuity at the transition point from the region below to the one above. The model has 11 parameters. A parameter extraction program has been developed for this model, which fits the measured data to extract the values of the 11 parameters. The fitting error is within 3 percent for nine orders of magnitude of current variation, which demonstrates the accuracy of this model. This model has been implemented in SPICE2. Benchmark tests indicate no convergence problems or speed penalty compared with the modified Shichman-Hodges model used in SPICE2. This indicates the simplicity and efficiency of this new current model. Large circuits (7,000 elements) have been simulated to quantify the improvements in the accuracy of circuit simulations. The results are very encouraging and illustrate the importance of including subthreshold components in the current models. For example, in a dRAM sense amplifier, simulation without subthreshold current predicts a V_T mismatch tolerance two to three times that of measured results, while simulation with subthreshold current predicts a V_T mismatch tolerance very close to measured results.

A. FORMULATION OF THRESHOLD VOLTAGE EQUATION

For short-channel MOSFETs, the substrate depletion charge is not totally controlled by the gate. Part of the depletion charge is controlled by the drain. Using this basic concept of charge sharing, we can modify the threshold equation to include this effect. By applying the charge conservation principle, we obtain

$$Q_G + Q_C + Q_B = 0 \tag{161}$$

where Q_G is the total charge on the gate, Q_C is the total channel mobile charge, and Q_B is the total ionized impurity in the depletion region (Figure 79).

Using the gradual channel approximation and the one-dimensional Poisson equation, we obtain

$$V_{GB} = V_{ox} + \psi_S + V_{FB} \tag{162}$$

$$V_{ox} = \frac{Q_G}{AC_{ox}} = \frac{-Q_C - Q_B}{AC_{ox}} \tag{163}$$

where V_{FB} is the flat-band voltage, ψ_s is the surface potential, and A is the area. The threshold voltage is given by setting $\psi_s = 2\phi_f - V_{BS}$ and $Q_C = 0$.

$$V_T = V_{FB} + 2\phi_f - \frac{Q_B}{AC_{ox}} \tag{164}$$

For short-channel MOSFETs, the full effect of Q_B on the threshold voltage is reduced [Equation (163)]. The threshold voltage equation for short-channel devices can be obtained by using an effective Q_B in Equation (164).

$$V_T = V_{FB} + 2\phi_f + BET\sqrt{2\phi_f - V_{BS}} \tag{165}$$

where BET is given by

$$BET = BE - DE\sqrt{2\phi_f + V_{DS} - V_{BS}} - \sqrt{2\phi_f} \tag{166}$$

In the above equation, BE is the body effect term for long channel devices, and BET is the simplified effective body effect term for short-channel devices.

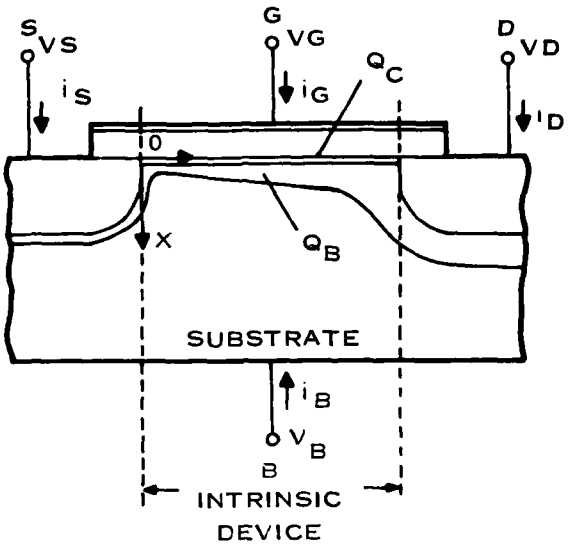


Figure 79. Schematic Diagram of a MOSFET

B. SUBTHRESHOLD CURRENT

The electron current-density equation is given by

$$J_n = q\mu_n nE + qD_n \nabla_n \tag{167}$$

where μ_n is the electron mobility and D_n is the electron diffusion constant. The first term in Equation (167) is the drift component and the second term is the diffusion component. From the Einstein relationship [$D_n = (kT/q)\,\mu_n$] and $E = -\nabla\psi$, we obtain

$$J_n = -q\mu_n n\nabla_{\phi n} \tag{168}$$

where ϕ_n is the electron quasi-Fermi level. We can see that Equation (168) contains both drift and diffusion components. Equation (168) can be rewritten for MOSFET as follows:

$$I_D = -w\mu_n q_c \frac{dVy}{dy} \tag{169}$$

From strong inversion assumption, the modified Shichman-Hodges electron surface density is given by

$$q_{c.msh} = -C_{ox}(V_{GS} - V_T - \alpha_x V_y) \tag{170}$$

where $\alpha_x = \alpha + \gamma (V_{GS} - V_T)$, α and γ are short-channel parameters [Equation (167)], and V_Y is the electron quasi-Fermi level at distance y measured along the channel from the source toward the drain. Substituting Equation (170) into Equation (169) and integrating from the source ($y = 0$, $V_y = 0$) either to the drain ($y = L$, $V_y = V_D$) in the linear region or to the saturation point ($y = L - \Delta L$, $V_y = V_{Dsat}$) in the saturation region, we obtain the modified Shichman-Hodges current model $I_{D.msh}$.

$$I_{D.msh} = \begin{cases} \alpha_x \beta_n C_{ox} [2(V_{GS} - V_T) V_{DS} - \alpha_x V_{DS}^2] & V_{GS} > V_{Gsat} \quad (171) \\ \beta_n C_{ox} (V_{GS} - V_T)^2 \left[1 + \lambda \left(\frac{\alpha}{\alpha_x}\right)^2 (V_{DS} - V_{Dsat})\right] & V_{Gsat} \geq V_{GS} > V_T \quad (172) \\ 0 & V_T \geq V_{GS} \quad (173) \end{cases}$$

where

$$V_{Dsat} = \frac{V_{GS} - V_T}{\alpha_s} \tag{174}$$

$$V_{Gsat} = V_T + \alpha_s V_{Ds} \tag{175}$$

$$\beta_n = \frac{(W - W_R)\,\mu_n}{(L - L_R)\,\alpha_s} \tag{176}$$

and

$$\mu_n = \frac{\alpha_s\,\mu_{no}}{1 + \theta\,(V_{GS} - V_T)} \tag{177}$$

W_R and Δ_R are the width and length reduction factors and λ is the channel length modulation parameter.

Even though Equation (169) contains both drift and diffusion components, the current I_D obtained by using Equations (169) and (170) does not have a subthreshold component as shown in Equation (173). The problem is with Equation (170). Equation (171) is based on a strong inversion assumption. This assumption gives a zero mobile charge density in the subthreshold region which, in turn, results in a zero subthreshold current. To resolve this problem, a more accurate mobile charge density representation is needed. The small but finite subthreshold mobile charge density can be obtained by solving the Poisson equation. The actual mobile charge density can be approximated by adding this small subthreshold mobile charge density to the mobile charge density given by Equation (170). The subthreshold mobile charge density can be obtained iteratively as follows. First, the total mobile charge density Q_c is assumed to be 0 in the subthreshold region. Substituting Equation (162) into Equation (163) and using the effective Q_B, we obtain

$$V_{GB} - \psi_s - V_{FB} = \frac{-Q_{B,eff}}{AC_{ox}} \tag{178}$$

where

$$\frac{-Q_{B,eff}}{AC_{ox}} = BET\sqrt{\psi_s}$$

From Equation (178), the surface potential ψ_s is given by

$$\psi_s = V_{GS} - V_{BS} - V_{FB} + \frac{BET^2}{2}\left\{1 - \sqrt{1 + \frac{4}{BET^2}(V_{GS} - V_{FB} - V_{BS})}\right\} \tag{179}$$

The electron carrier density is given by

$$\eta_p = \eta_{po}\exp^{\beta(\psi + V_{Bs})} \tag{180}$$

Using Equations (179) and (180), we obtain the subthreshold electron surface density

$$q_{c,sub} = -q\int_0^\infty \eta_p dx \tag{181}$$

$$= -q\int_{\psi_s}^0 \frac{\eta_p\,d\psi}{\frac{d\psi}{dx}} \tag{182}$$

In the subthreshold region, $d\psi/dx$ can be approximated by

$$\frac{d\psi}{dx} \approx -\frac{\sqrt{2}kT}{qL_D}\sqrt{\beta\psi} \tag{183}$$

where L_D is the extrinsic Rebye length and $\beta = q/kT$.

Substituting Equation (183) into Equation (182), we obtain

$$q_{c,sub} = \frac{\epsilon_s}{\sqrt{2}L_D} e^{\beta(V_{BS} - 2\phi_f)} \int_0^{\psi_s} \frac{\exp^{\beta\psi}}{\sqrt{\beta\psi}}\, d\psi \tag{184}$$

Let $p = \sqrt{\beta\psi}$ and changing a variable, Equation (184) can be rewritten as

$$q_{c,sub} = \frac{-\sqrt{2}\epsilon_s}{\beta L_D} e^{\beta(V_{BS} - 2\phi_f)} \int_0^{\sqrt{\beta\psi_s}} \exp^{p^2}\, dp \tag{185}$$

For the current range of interest ($I_D \geq 10^{-12}$ A), Equation (185) can be approximated by

$$q_{c,sub} = \frac{-\sqrt{2}\epsilon_s A_o}{\beta L_D} \exp^{N_G\beta(V_{BS} - 2\phi_f + \psi_s)} \tag{186}$$

where $A_o \approx 0.3$ and $N_G \approx 1.0$. N_G is used for the approximation of the integral and also to represent the uncertainty of the device temperature.

The total charge density can be obtained by adding Equation (186) to Equation (170).

$$\begin{aligned} q_c &= q_{c,msh} + q_{c,sub} \\ &= -C_{ox}(V_{GS} - V_T - \alpha_x V_y) - \frac{\sqrt{2}\epsilon_s A_o}{\beta L_D} \exp^{N_G\beta(V_{BS} - 2\phi_f + \psi_S)} \end{aligned} \tag{187}$$

The total current can be obtained by substituting Equation (187) into Equation (169)

$$I_D = I_{D,msh} + I_{D,sub} \tag{188}$$

and

$$\begin{aligned} I_{D,sub} &= \frac{\sqrt{2}\mu_n\epsilon_s (W - W_R) A_o}{\beta L_D (L - L_R)} \int_0^{V_{DS}} \exp^{N_G\beta(V_{BS} - 2\phi_f + \psi_s)\, dV_y} \\ &= \frac{\sqrt{2}\mu_n\epsilon_s (W - W_R) A_o}{\beta L_D (L - L_R)} \exp^{N_G\beta(\psi_s - 2\phi_f + V_{BS})} \\ &= \beta_S \exp^{N_G \times \beta(\psi_s - 2\phi_f + V_{BS})} (1 - \exp^{-N_G \times \beta \times V_{DS}}) \end{aligned} \tag{189}$$

where

$$\beta_S = \frac{\sqrt{2}\mu_n\epsilon_S (W - W_R)}{N_G \beta L_D (L - L_R)} \tag{190}$$

To obtain a computationally efficient model, Equation (189) must be simplified. First, for $V_{GS} \geq V_T$, let $\psi_S = 2\phi_n$. Note that this is possible because we have consistent V_T and ψ_S equations [Equations (165) and (179)]. When V_{GS} is equal to V_T, Equation (179) will give a ψ_S equal to $2\phi_n$. Second, $I_{D\,sat}$ is small compared to $I_{D\,max}$ in the above-threshold region; let μ_n in Equation (190) be a constant even in the above-threshold region. Equation (190) now can be rewritten as

$$I_{D\,sub} = \begin{cases} \beta_S(1 - \exp^{\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot}) & V_{GS} \geq V_T \quad (191) \\ \beta_S \exp^{\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot} (1 - \exp^{\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot\,\cdot}) & V_T < V_{GS} \quad (192) \end{cases}$$

C. DISCUSSION AND RESULTS

This current model contains both components above and below threshold. I_D is given by the addition of $I_{D\,max}$ and $I_{D\,sub}$, and current continuity is guaranteed. For $V_{GS} \geq V_T$ and V_{DS} greater than several kT/q, $I_{D\,sub}$ is equal to β_S, which is a constant. For $V_{GS} < V_T$, $I_{D\,max}$ is equal to zero. This simplicity ensures the computational efficiency of the model. A parameter extraction program is developed for this model that fits the measured data to extract the values of the 11 parameters. The fitting error is within 3 percent for nine orders of magnitude of current variation. An overlay of the experimental data and the computed curve for a 1.5-μm MOSFET is shown in Figure 80. The values of the extracted model parameters are given in Table 7.

This model has been implemented in SPICE2 and has been tested extensively against static and dynamic MOSFET circuits including sRAMs, dRAM sense amplifiers, and other MOS VLSI circuits. Part of the CPU time comparison results is given in Table 8. No speed penalty or convergence problems exist. The simulation results also indicate the importance of including the subthreshold component in the current models. Figure 81 shows a simplified schematic diagram of a dRAM sense amplifier. After selecting the storage cell and the opposite dummy cell, the differential signals are stored on capacitors c_1 and c_2. Consider the case when V_1 is low, V_2 is high, ϕ_1 is low, and a ΔV_T mismatch exists between the two cross-coupled transistors M_1 and M_2. Without the subthreshold component, the ΔV_T tolerance is equal to[74]

$$\frac{(V_2 - V_1)}{\left(1 + \dfrac{C_S}{C_S}\right)}$$

With the subthreshold component, there will be a subthreshold current flowing from node 2 through transistors M_1 and M_2 to node 1. This current will reduce the differential signal between nodes 1 and 2. Therefore, the ΔV_T tolerance will be smaller than

$$\frac{(V_2 - V_1)}{1 + \left(\dfrac{C_S}{C_S}\right)}$$

Simulation results confirm the above analysis. For the particular simulated dRAM sense amplifier, simulation without subthreshold current predicts a 90-mV ΔV_T tolerance, while simulation with subthreshold current predicts a 45-mV ΔV_T tolerance. The measured ΔV_T tolerance is between 30 and 50 mV.

[74]T. Furuyana, S. Saito, and S. Fujii, "A New Sense Amplifier Technique for VLSI Dynamic RAMs," *IEDM Technical Digest* (1981).

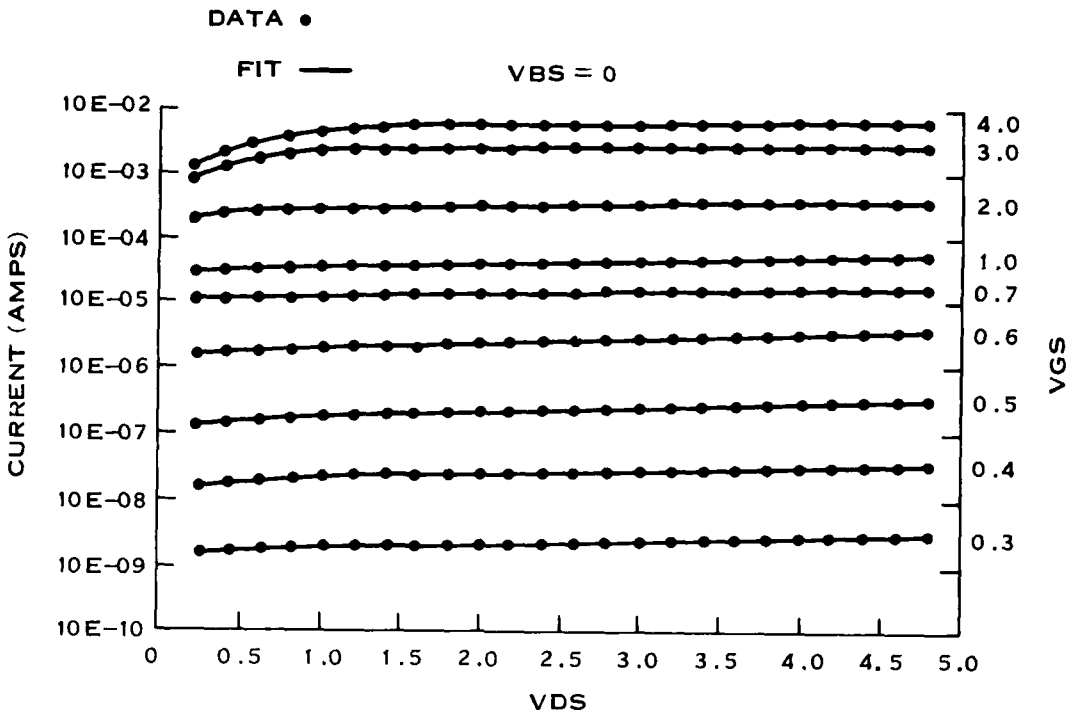


Figure 80. Overlay of Experimental Data and Computed Curve

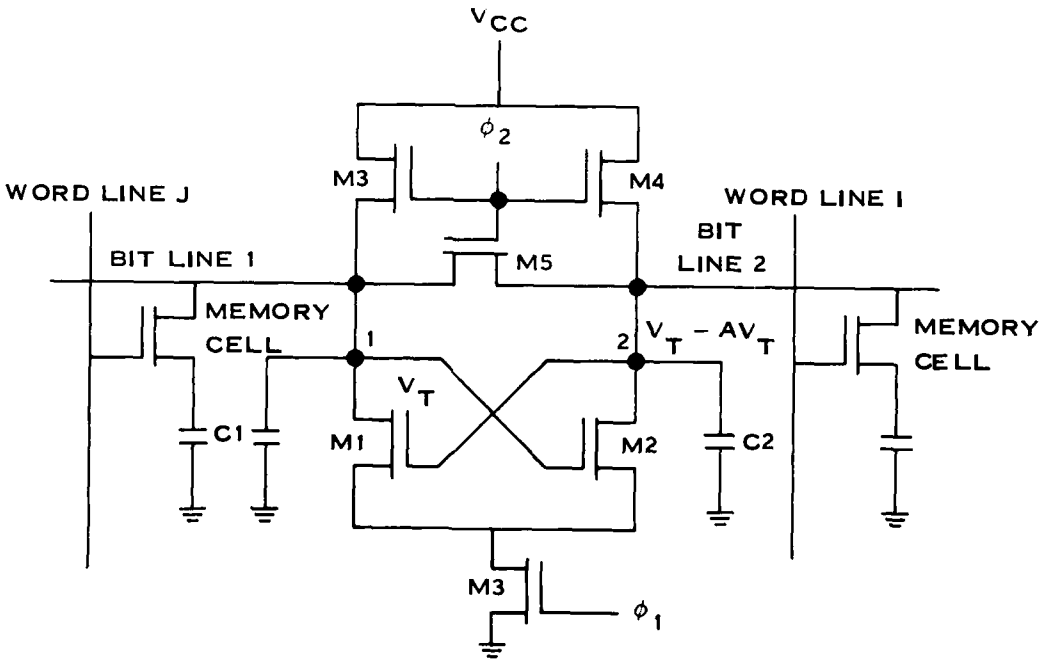


Figure 81. Simplified Schematic Diagram of a dRAM Sense Amplifier

TABLE 7. VALUES OF ELEVEN MODEL PARAMETERS

Parameter	Value
β_n	0.12230525 E − 03
V_{FB}	−0.72497901 E + 00
ϕ_f	0.38000000 E + 00
B_E	0.63799526 E + 00
α	0.10528654 E + 01
θ	0.23623521 E + 00
λ	0.10911962 E + 00
γ	0.11990967 E + 00
D_E	0.33129107 E − 01
β_S	0.97377110 E − 06
N_G	0.83509249 E + 00

TABLE 8. CPU TIME COMPARISON BETWEEN NEW MODEL AND MODIFIED SHICHMAN-HODGES MODEL (MSH)

Circuit	dRAM Sense Amplifier (102 MOSFETs)	sRAM (171 MOSFETs)
MSH Model Transient Analysis CPU Time in Seconds (Number of Iterations)	1198.94 (2444)	1563.62 (734)
New Model Transient Analysis CPU Time in Seconds (Number of Iterations)	1266.34 (2446)	1484.27 (738)

SECTION X

MOSFET CAPACITOR MODEL FOR SPICE2

A. INTRODUCTION

Charge conservation in SPICE is crucial for simulation of MOS circuits such as dynamic RAMs and switched capacitors. Meyer's capacitance model,[75] which is presently used in SPICE2, does not guarantee conservation of charge, and thus circuit simulation results can be inaccurate. Recent attempts to resolve the charge-conservation problem have been published in the literature.[76,77] These efforts have assumed that charge conservation may be achieved through more accurate representations of the device physics. In Reference 76, nonreciprocal capacitances were introduced, and the inclusion of source- and drain-bulk capacitances was considered to be required for charge conservation. In Reference 77, a four-terminal equivalent circuit was introduced that is supposed to conserve charge.

We have found that nonconservation of charge in SPICE2 is independent of device physics and is a result of the way the charge is numerically evaluated using capacitance equations. An example is given to illustrate the basic cause of nonconservation of charge. Some basic numerical methods used in circuit analysis are reviewed first.

B. NUMERICAL METHODS

The key elements of the derivation of the charge-conserving capacitance model presented in this report are based on the numerical techniques used for the implementation of the model in SPICE2. These techniques are reviewed in this subsection. Readers who do not feel the need for such a review should proceed to Subsection X.C.

1. *Numerical Integration—Trapezoidal Algorithm*

Many different algorithms for numerical integration are used within SPICE2. The section of SPICE2 program code where nonconservation of charge occurs uses the trapezoidal method, which is reviewed in this subsection.

To make discrete the time domain solution of a variable x (Figure 82), one may use the simple recursion formula to integrate the time evolution of x in the time period $(t_{n+1} - t_n)$,

$$x_{n+1} = x_n + (t_{n+1} - t_n)\frac{(\dot{x}_{n+1} + \dot{x}_n)}{2} \tag{193}$$

In the above expression, the time derivatives $\dot{x}_{n+1} + \dot{x}_n$ have been averaged to approximate the mean value derivative. SPICE2 uses variable time intervals so that

$$(t_n - t_{n-1}) \neq (t_{n+1} - t_n) \tag{194}$$

For this discussion, however, assume that all time intervals are equal to h. Thus,

$$t_{n+1} - t_n = h \tag{195}$$

[75]J.E. Meyer, "MOS Models and Circuit Simulation," *RCA Rev.* **32** (March 1971), p. 42.

[76]D.E. Ward and R.W. Dutton, "A Charge-Oriented Model for MOS Transistor Capacitances," *IEEE J. Solid-State Circuits* **13** (October 1978), p. 703.

[77]Y.A. El-Mansy and A.R. Boothroyd, "A General Four-Terminal Charging-Current Model for the Insulated-Gate Field-Effect Transistor–I," *Solid State Electronics* **23** (1980), p. 405.

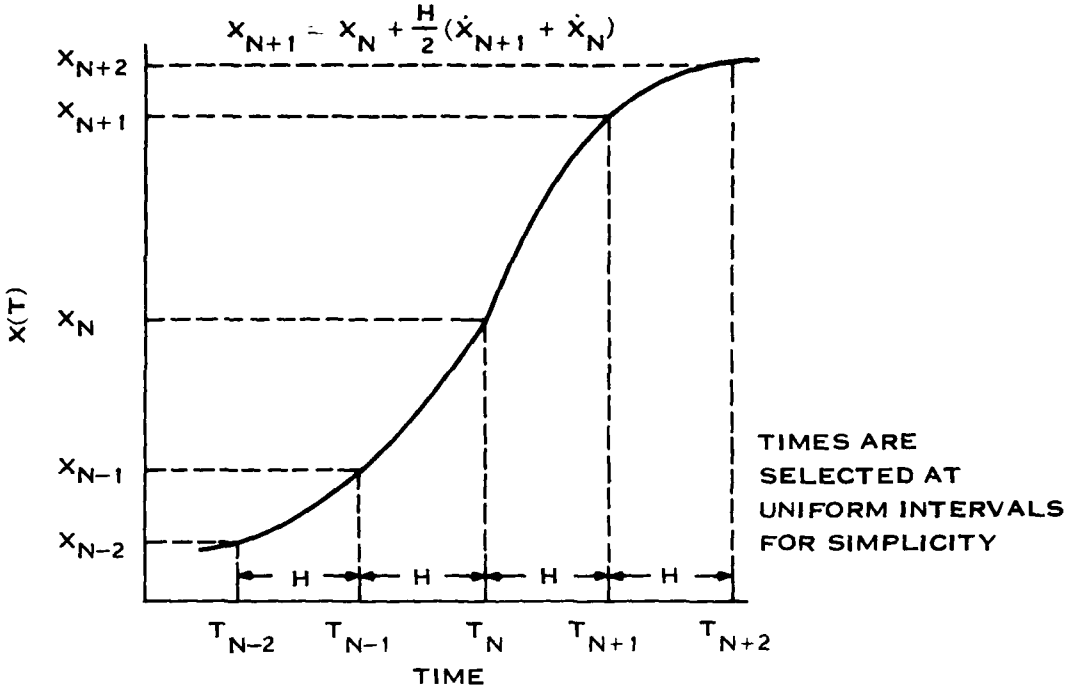


Figure 82. Function X(+) Numerically Integrated Using the Trapezoidal Method

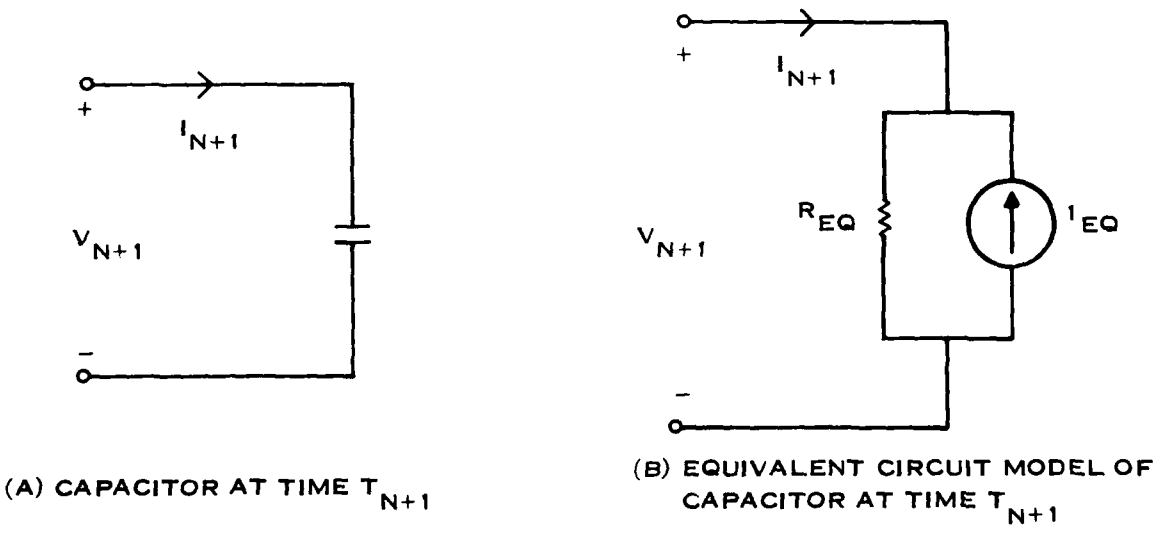


Figure 83. Model Represented by Parallel Resistor and Source

and Equation (193) becomes

$$x_{n+1} = x_n + \frac{h}{2}(\dot{x}_{n+1} + \dot{x}_n) \tag{196}$$

2. Associated Discrete Circuit Model for a Capacitor-Companion Model

The numerical discretization of this differential equation results in a difference equation that can be represented by the parallel combination of a resistor and a current source,[78] as shown in Figure 83. This representation may be derived as follows. The voltage V_n+1 at time t_n+1 is related to the voltage at time t_n by Equation (196):

$$V_{n+1} = V_n + \frac{h}{2}(\dot{V}_{n+1} + \dot{V}_n) \tag{197}$$

Substituting the branch relationship for a capacitor

$$I = C\dot{V} \tag{198}$$

into Equation (197) yields

$$V_{n+1} = V_n + \frac{h}{2}\left(\frac{I_{n+1}}{C_{n+1}} + \frac{I_n}{C_n}\right) \tag{199}$$

and solving for I_{n+1} gives

$$I_{n+1} = \left(\frac{2C_{n+1}}{h}\right) V_{n+1} - \left(\frac{C_{n+1}}{C_n} I_n + \frac{2}{h} C_{n+1} V_n\right) \tag{200}$$

Equation (200) directly represents the current I_n+1 and voltage V_n+1 through the capacitor in terms of their values I_n and V_n at time t_n. I_n+1 and V_n+1 are the unknowns to be calculated, and inspection of Equation (200) suggests that we may define an equivalent resistance R_{eq} as

$$R_{eq} = \frac{h}{2C_{n+1}} \tag{201}$$

The values of I_n and V_n in Equation (200) were determined in the t_n time step evaluation and are constants for the t_n+1 time step evaluation. Therefore, the terms in the second set of parentheses in Equation (200) can be represented by a current source

$$I_{eq} = \frac{C_{n+1}}{C_n} I_n + \frac{2}{h} C_{n+1} V_n \tag{202}$$

If the capacitor is linear

$$C_n = C_{n+1} \tag{203}$$

then R_{eq} and I_{eq} have been uniquely determined and the capacitor has been successfully made discrete. If the capacitor is nonlinear

$$C_n \neq C_{n+1} \tag{204}$$

[78]L.O. Chua and P. Lin, *Computer-Aided Analysis of Electronic Circuits—Algorithms and Computational Techniques*, Prentice-Hall, Inc.(Englewood Cliffs, N.J., 1975).

then the Newton-Raphson iteration must be used to determine C_{n+1}. The discussion of the Newton-Raphson iteration to determine C_{n+1} is given in Subsection E. Subsection C presents examples with nonlinear capacitors, but C_{n+1} will be known *a priori*.

C. CHOICE OF STATE VARIABLE—TWO EXAMPLES

In general, either charge or voltage can be chosen as the state variable for a capacitor. From a computational point of view, it is advantageous to select charge as the state variable because it can be shown to result in less error propagation. SPICE2 uses charge as the state variable but calculates the charge from

$$Q = \int C(V)\, dV \tag{205}$$

rather than from an explicit analytic expression for the charge. The examples in this section illustrate that, for nonlinear capacitors, charge *must* be chosen as the state variable. These examples do not explicitly show how nonconservation of charge occurs in SPICE2 but do provide insight into the problem.

Both examples analyze the circuit in Figure 84(a), which consists of a constant voltage source, a nonlinear capacitor C_1, and a linear capacitor C_2. The nonlinear capacitor C_1 can be envisioned as a metal tube through which there is an insulating rod of sufficient length that parasitic capacitances between points A and B can be neglected. Part of this rod is plated with metal, as indicated by the shaded portion of the rod, and for $t < 0$, only part of the shaded region is within the cylinder; therefore, a capacitance of $C_1(0^-)$ results. At time $t = 0$, voltage V_3 activates the solenoid, and the plated region of the insulating rod is thus pushed entirely within the insulating cylinder for $t > 0$, so C_1 becomes $C_1(0^+)$. Thus, as illustrated in Figure 84(c), the capacitor C_1 has values

$$\begin{aligned} C_1 &= C_1(0^-) \text{ for } t < 0 \\ C_1 &= C_1(0^+) \text{ for } t > 0 \end{aligned} \tag{206}$$

Note that the voltage V_3 that causes this change is independent of both V_1 and V_2, the terminal voltages of C_1. This problem is simple enough to be analytically solved for $V_2(0^+)$ in terms of V_1 and $V_2(0^-)$:

$$V_2(0^+) = \frac{C_1(0^+) - C_1(0^-)}{C_1(0^+) + C_2} V_1 + \frac{C_1(0^-) + C_2}{C_1(0^+) + C_2} V_2(0^-) \tag{207}$$

Figure 84(b) is a discrete representation of the actual circuit in Figure 84(a), which used the companion model developed in the previous section. The following two examples analyze the circuit of Figure 84. The first example uses voltage as the state variable, and the second uses charge as the state variable.

1. Example 1—Voltage as State Variable

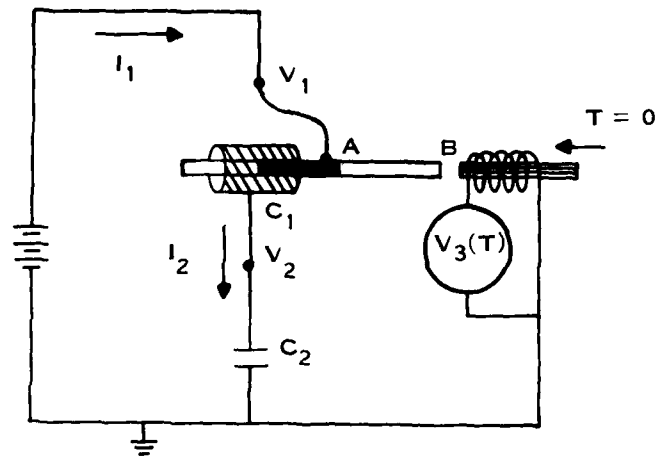
The companion model developed in Subsection B.2 uses voltage as the state variable. Reproducing that derivation will point out the problem with this approach.

The trapezoidal method using voltage as the state variable is written as

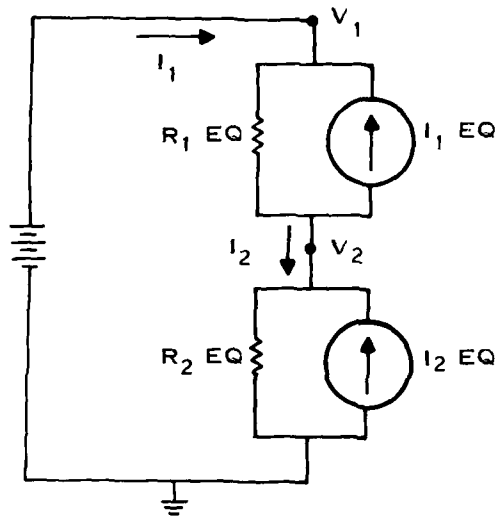
$$V_{n+1} = V_n + \frac{h}{2}(\dot{V}_{n+1} + \dot{V}_n) \tag{208}$$

Substituting the branch relationship for a capacitor

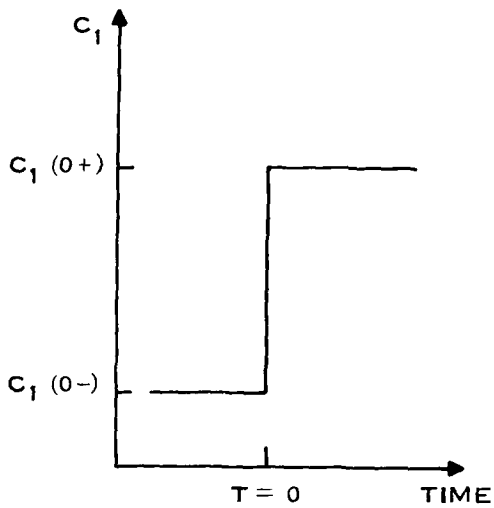
$$I = C\dot{V} \tag{209}$$



(A) CIRCUIT USED IN EXAMPLES 1 AND 2



(B) EQUIVALENT CIRCUIT FOR EXAMPLES 1 AND 2



(C) VALUE OF CAPACITOR C_2 VERSUS TIME

Figure 84. Actual and Discrete Circuits With Capacitance Versus Time

into Equation (208) and solving for I_{n+1} yields

$$I_{n+1} = \left(\frac{2C_{n+1}}{h}\right) V_{n+1} - \left(\frac{C_{n+1}}{C_n} I_n + \frac{2}{h} C_{n+1} V_n\right) \tag{210}$$

Using Equation (210), we can write for the circuit of Figure 84(a)

$$I_1(0^+) = \frac{2C_1(0^+)}{h} V_{12}(0^+) - \left[\frac{C_1(0^+)}{C_1(0^-)} I_1(0^-) + \frac{2}{h} C_1(0^+) V_{12}(0^-)\right] \tag{211}$$

and

$$I_2(0^+) = \frac{2C_2}{h} V_2(0^+) - \left[I_2(0^-) + \frac{2}{h} C_2 V_2(0^-)\right] \tag{212}$$

where

$$V_{12} = V_1 - V_2 \tag{213}$$

These equations can be solved by requiring

$$I_1(0^+) = I_2(0^+) \tag{214}$$

and with a dc voltage source and C_1 constant for $t < 0$,

$$I_1(0^-) = I_2(0^-) = 0 \tag{215}$$

This yields

$$V_2(0^+) = V_2(0^-) \tag{216}$$

thus

$$I_1(0^+) = I_2(0^+) = 0 \tag{217}$$

which is the wrong solution because a displacement current will flow when C_1 changes values.

This anomalous result can be traced back to the use of the branch relationship of Equation (209), which should have been written as

$$I = \frac{dQ}{dt} = C_{DC} \dot{V} + \dot{C}_{DC} V = C_{SS} \dot{V} \tag{218}$$

A distinction has been made in Equation (218) between a physical capacitor, C_{DC}, and a small signal capacitance, C_{SS}. A physical capacitor is defined in terms of area, distance, and a dielectric constant, and for a parallel plate capacitor the capacitance is

$$C_{DC} = \frac{\epsilon A}{d} \tag{219}$$

A small signal capacitance is defined as

$$C_{SS} = \frac{\partial Q}{\partial V} \tag{220}$$

In Figure 84(a), the physical capacitor between points 2 and 3 can be neglected because the distance AB can be made very large. The small signal capacitance between points 2 and 3, however, cannot be neglected because

$$I_1 = \frac{dQ_1}{dt} = \frac{\partial Q_1}{\partial V_{12}} \dot{V}_{12} + \frac{\partial Q_1}{\partial V_{32}} \dot{V}_{32} \tag{221}$$

$$= C_{12,SS} \dot{V}_{12} + C_{32,SS} \dot{V}_{32} \tag{222}$$

and $C_{32,SS}$ is independent of the distance between A and B. If we examine the entire circuit in detail, we will find $C_{12,SS}$, $C_{21,SS}$, $C_{13,SS}$, $C_{31,SS}$, $C_{23,SS}$ and $C_{32,SS}$ as illustrated in Figure 85. It is important to recognize that these small signal capacitances do not physically exist as capacitors but are equivalent circuit representations of $C_{1,DC}$, allowing for the transfer of energy between the mechanical motion of the solenoid and

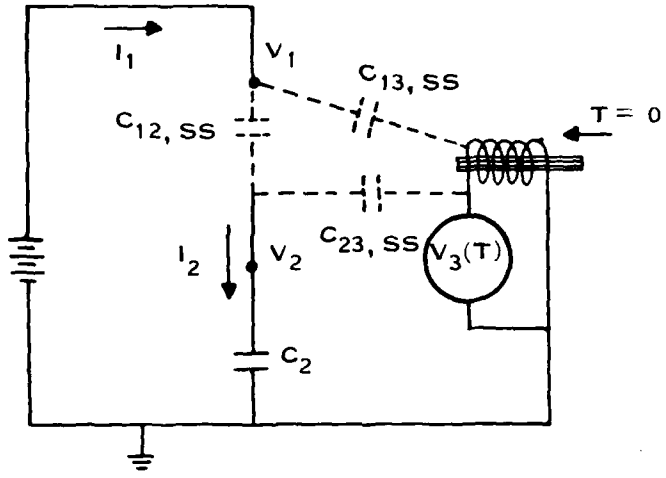


Figure 85. Small Signal Equivalent Circuit Model that Accounts for Effects of C, in Figure 84(a)

the change of potential at node 2 because of the change in $C_{1,DC}$. We cannot use this equivalent circuit to solve this example because

$$\dot{C}_{1,DC} = \infty \tag{223}$$

and thus the equivalent circuit small signal capacitance cannot be defined.

The result in Equation (217) neglects the $\dot{C}V_V$ term of Equation (209), and $\dot{C}_V$ represents the physical mechanism resulting in a displacement current.

2. Example 2—Charge as State Variable

The same problem may be solved using charge Q as the state variable. From Equation (196) we can write for the trapezoidal method

$$\begin{aligned} Q_{n+1} &= Q_n + \frac{h}{2}(\dot{Q}_{n+1} + \dot{Q}_n) \\ &= Q_n + \frac{h}{2}(I_{n+1} + I_n) \end{aligned} \tag{224}$$

If we use the branch relationship for a capacitor in terms of charge (which is the fundamental definition of capacitance)

$$Q = CV \tag{225}$$

from Equation (224) we may write

$$I_{n+1} = \frac{2}{h} C_{n+1} V_{n+1} - \frac{2}{h} C_n V_n - I_n \tag{226}$$

Thus, the discrete model in Figure 83 has

$$R_{eq} = \frac{h}{2C_{n+1}}$$

and

$$I_{eq} = -\left(\frac{2}{h} C_n \dot{V}_n + I_n\right) \tag{227}$$

Reworking Example 1 using charge as the state variable and using Equation (227), we can write

$$I_h(0^+) = \frac{2}{h} C_1(0^+) V_{12}(0^+) - \frac{2}{h} C_1(0^-) V_{12}(0^-) - I_1(0^-) \tag{228}$$

and

$$I_2(0^+) = \frac{2}{h} C_2 V_2(0^+) - \frac{2}{h} C_2 V_2(0^-) - I_2(0^-) \tag{229}$$

This set of equations can be solved by requiring

$$I_1(0^+) = I_2(0^+) \tag{230}$$

and

$$I_1(0^-) = I_2(0^-) = 0 \tag{231}$$

which yields

$$V_2(0^+) = \frac{C_1(0^+) - C_1(0^-)}{C_1(0^+) + C_2} V_1 + \frac{C_1(0^-) + C_2}{C_1(0^+) + C_2} V_2(0^-) \tag{232}$$

The result in Equation (232) is the same as that obtained from an analytic solution of the problem.

It can now be seen that the selection of voltage as the state variable is not the proper choice because the branch relationship for the capacitor involves the displacement current and time-varying capacitances, the time derivatives of which cannot be defined for this example. When charge is selected as the state variable, the branch relationship for the capacitor involves charge and does not require the time derivatives of the capacitors. Thus, charge is the proper state variable to select to obtain the correct solution.

D. NONCONSERVATION OF CHARGE IN SPICE2

The fact that charge is not conserved in SPICE2 for circuits with various time-variant capacitor elements has been known for many years. We illustrate this shortcoming with a circuit for which SPICE2 does not conserve charge. Figure 86 is the schematic of a circuit simulated using SPICE2 and is designed to resemble the circuit in Figure 84, which was analyzed in the previous examples. The nonlinear capacitor C_1 in Figure 84 is represented by C_{GS} of the MOSFET in Figure 86. The value of C_{GS} will depend on the drain and substrate terminal voltages. These terminal voltages are cycled as shown in Figure 87 so that after one complete cycle of 100 ns, C_{GS} should be back to its starting value. Thus, each successive cycle should generate the same output voltage waveform. Figure 88 shows the results of the SPICE2

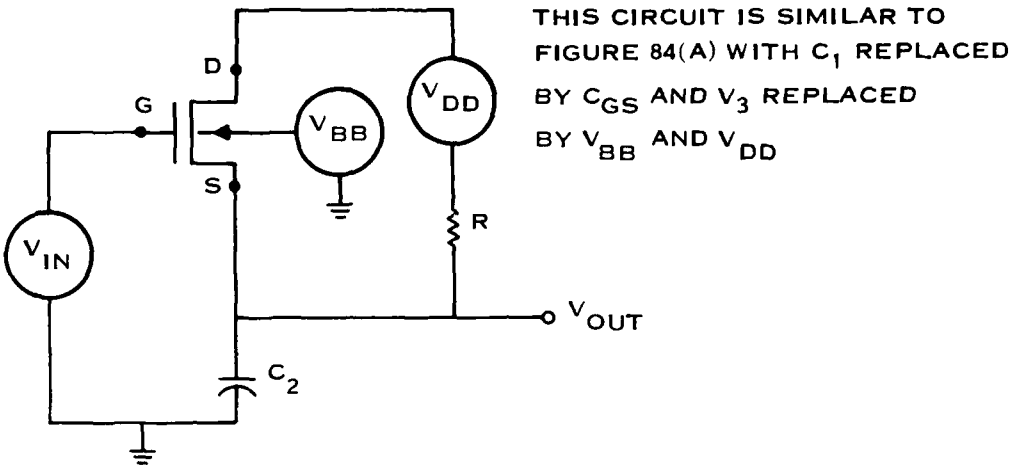


Figure 86. Circuit Schematic Simulated in SPICE2 to Show Nonconservation of Charge

simulation of this circuit for two different error tolerance conditions for the program. At every iteration or time, the program must meet a current tolerance, a voltage tolerance, and a charge tolerance. If the tolerances are not properly chosen, the accumulated errors will appear as nonconservation of charge, even for a linear capacitor. As can be seen from Figure 88, V_{OUT} drops for each successive cycle, even when the tolerances are set very tight. This cyclical reduction in V_{OUT} is a result of nonconservation of charge, which cannot be eliminated by restricting the tolerances.

Nonconservation of charge occurs because SPICE2 calculates charge from

$$Q = \int_{V_{12}(t_1)}^{V_{12}(t_2)} C_{12}(V_{12})\, dV_{12} \tag{233}$$

where V_{12} is the voltage across nodes 1 and 2, the terminal nodes of the capacitor. If the value of the capacitor C_{12} depends on a voltage such as V_3 in the example of Subsection C, the integral in Equation (233) will not properly account for changes in charge caused by changes in C_{12} with changes in V_{23}.

This can most easily be illustrated by examining a specific example. Let us assume a capacitor C_{12} has the functional dependence on V_{12} and V_{23} as shown in Figure 89. If we start at point 1 in Figure 89 at time t_1, charge $Q_1 = 0$, capacitance C_{12} and $V_{12} = V_{23} = 0$ and then follow the path 1, 2, 3, 4, 5, 6, 7, we should end at point 7 with

$$Q_7 = Q_1 = 0 \tag{234}$$

because points 1 and 7 are the same location and $V_{12} = 0$. Now let us examine this path in detail.

$$Q_{12} = \int_{V_{12}(t_1)}^{V_{12}(t_2)} C_{12}(V_{12})\, dV_{12} \neq 0 \tag{235}$$

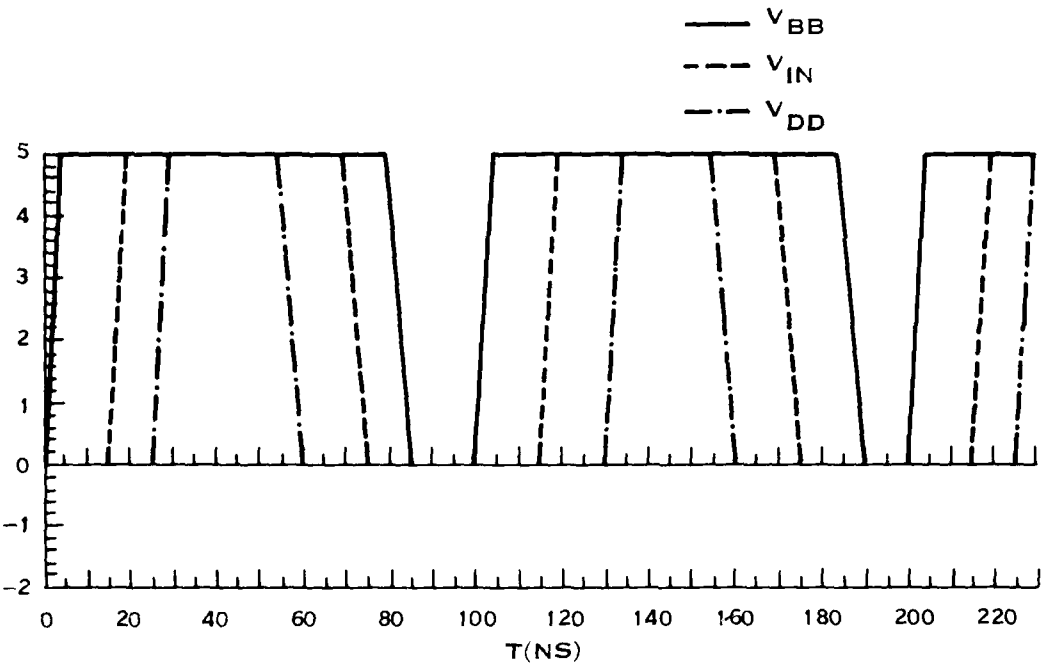


Figure 87. Voltage Supply Waveforms from SPICE2 for the Circuit of Figure 86

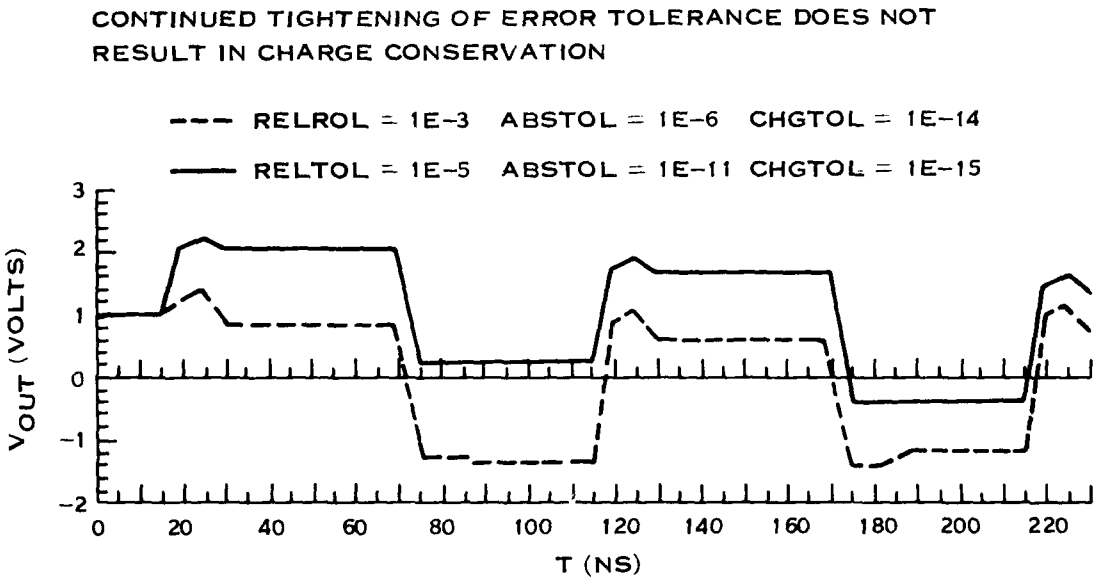


Figure 88. Output Waveform from SPICE2 Showing Nonconservation of Charge for Circuit of Figure 86

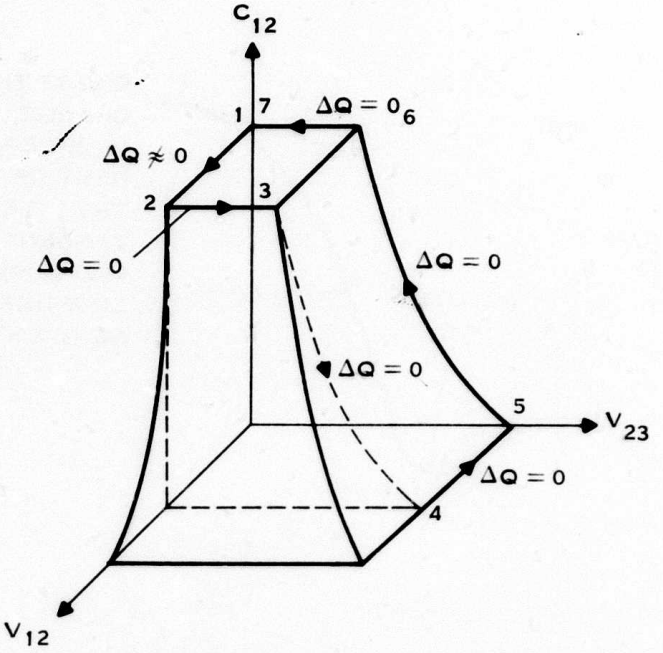


Figure 89. Path-Dependent Nature of Charge for Arbitrary Capacitor with Capacitance Depending on Voltage Other Than Its Own

because V_{12} is changing and C_{12} is nonzero.

$$Q_{23} + Q_{34} = \int_{V_{12}(t_2)}^{V_{12}(t_3)} C_{12}(V_{12})\, dV_{12} + \int_{V_{12}(t_3)}^{V_{12}(t_4)} C_{12}(V_{12})\, dV_{12} = 0 \tag{236}$$

because

$$V_{12}(t_2) = V_{12}(t_3) = V_{12}(t_4) \tag{237}$$

$$Q_{45} = \int_{V_{12}(t_4)}^{V_{12}(t_5)} C_{12}(V_{12})\, dV_{12} = 0 \tag{238}$$

because

$$C_{12}(V_{12}) = 0 \tag{239}$$

$$Q_{56} + Q_{67} = \int_{V_{12}(t_5)}^{V_{12}(t_6)} C_{12}(V_{12})\, dV_{12} + \int_{V_{12}(t_6)}^{V_{12}(t_7)} C_{12}(V_{12})\, dV_{12} = 0 \tag{240}$$

because

$$V_{12}(t_5) = V_{12}(t_6) = V_{12}(t_7) \tag{241}$$

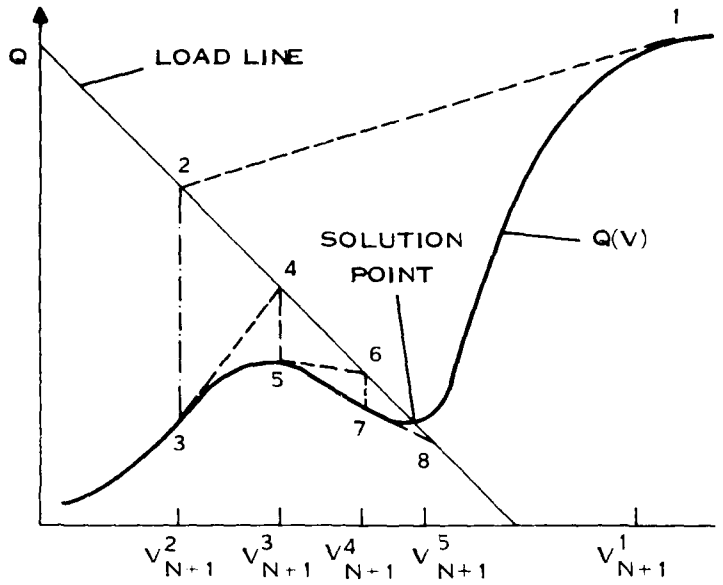


Figure 90. Schematic Representation of Newton-Raphson Iteration in SPICE2 to Determine Solution Point at Time

We now have

$$Q_7 = Q_1 + Q_{12} + Q_{23} + Q_{34} + Q_{45} + Q_{56} + Q_{67} \tag{242}$$

$$Q_7 = Q_{12} \neq 0 \tag{243}$$

so

$$Q_1 \neq Q_7 \tag{244}$$

and charge has not been conserved. This is because the changes of $C_{12}(V_{12})$ with changes in V_{23} are not included in the integral of Equation (233).

E. NEWTON-RAPHSON ITERATION AND THE INSIGNIFICANCE OF CAPACITANCE

Other than evaluating the charge, the only other use of capacitance in SPICE2 is in the Newton-Raphson iteration to determine V_{n+1}. If the capacitance is nonlinear, the Newton-Raphson iteration will determine the value of capacitance as well as V_{n+1}.

Considering a specific example as illustrated in Figure 90, charge is plotted as an arbitrary function of voltage. From Equation (224), developed from the trapezoidal method,

$$I_{n+1} = -I_n + \frac{2}{h}(Q_{n+1} - Q_n) \tag{245}$$

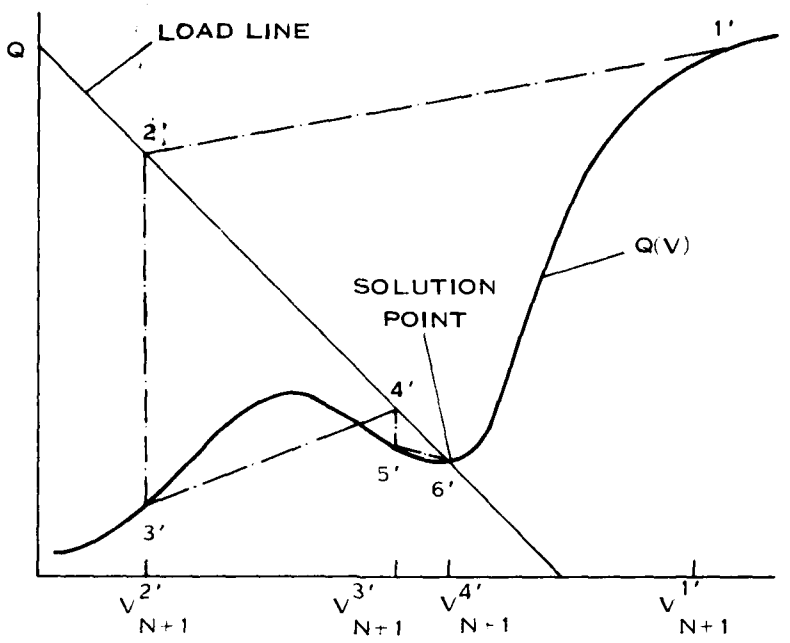


Figure 91. Schematic of Newton-Rachson Iteration in SPICE2 for Next Estimate of V_{AT1}

If we can find Q_{n+1}, we will know I_{n+1}. This is accomplished by estimating V_{n+1}^1, which is shown in Figure 90. The second estimation of V_{n+1} is generated by finding the intersection between the line tangent to point 1 and the circuit load line. This intersection occurs at point 2, which defines our second estimation, V_{n+1}^2. Continuing with this procedure, we can find the tangent line at point 3, and its intersection with the load line determines our third estimation for V_{n+1}. This iteration scheme can be continued until we are as close as desired to the actual solution point. Each time we find the tangent line, we use

$$C \equiv \frac{\partial Q}{\partial V} \tag{246}$$

The only use for capacitance in Newton-Raphson iteration is to determine the slope of the tangent line.

In numerical analysis, it is not necessary for the slope of the tangent line (and thus the capacitance) to be determined accurately to converge to the solution. This fact is illustrated in Figure 91, where instead of using the tangent line, a line with slope C/2 is used and convergence is still obtained. It is possible to determine the solution with no reference to the capacitance by using the bisection method. Thus, for a numerical analysis, the capacitance does not play a significant role.

F. CHARGE EQUATIONS FOR A MOSFET

We have shown that calculating the charge from

$$Q = \int C(V)\, dV \tag{247}$$

yields incorrect results for a MOSFET and that an accurate determination of capacitance is not required for convergence of the Newton-Raphson iteration. Indeed, when charge is the value that needs to be

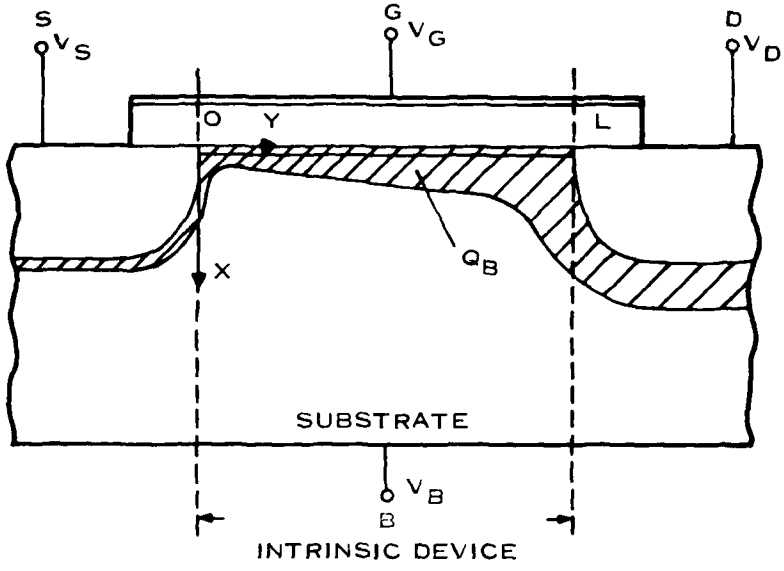


Figure 92. Region Defining Intrinsic Capacitance of MOSFET

accurately known, the capacitance approach can be abandoned in favor of deriving charge equations for use in SPICE2.

The MOSFET can be partitioned into intrinsic and extrinsic regions, as shown in Figure 92. The extrinsic region can be modeled by fixed capacitors representing the gate overlap caused by lateral diffusion of the source and drain plus p-n junction capacitors to represent the source and drain depletion layers. These extrinsic capcitances are either fixed or have values controlled only by their own terminal voltages, so the charge can be determined by integrating the capacitance over the terminal voltages.

Modeling of the intrinsic regions is more complicated because the capacitances are controlled by voltages other than their own terminal voltages. The charge equations must be continuous through all regions of operation to be useful for circuit simulation. The charge equations in the linear and saturation regions are derived from the dc model presented in Subsection IX.A. The equations in the subthreshold and accumulation regions are derived by solving the one-dimensional Poisson equation.[79,80] The charge equations for the subthreshold region have not yet been implemented in SPICE2 for the model presented in Section IX.

1. Linear Region $V_{GSAT} \leq v_{GS}$

The following definitions will be used: The values q_G, q_C, q_B represent the differential charge elements along the channel before taking the integral over source to drain voltage. These differential charge densities are then given by

$$\begin{aligned} q_G &= C_{ox}[V_{GS} - V_{FB} - 2\phi_F - V_y] \\ q_C &= -C_{ox}[V_{GS} - V_T - \alpha_x V_y] \\ q_B &= -C_{ox}[V_T - V_{FB} - 2\phi_F - (1 - \alpha_x)V_y] \end{aligned} \tag{248}$$

[79]H.K. Ihantola and J.M. Moll, "Design Theory of a Surface Field-Effect Transistor," *Solid-State Electronics*, 7 (1964), p. 423.

[80]S.M. Sze, *Physics of Semiconductor Devices*, John Wiley and Sons, Inc. (New York, 1969).

where

$$\alpha_x = \alpha + \gamma(V_{GS} - V_T) \tag{249}$$

$$V_{GSAT} = V_T + \alpha_x V_{DS}$$

$$\alpha = \text{alpha of Subsection IX.B}$$

$$\gamma = \text{gamma of Subsection IX.B}$$

and q_C is the mobile channel charge. Carrying out the integration in channel voltage yields

$$Q_G = WLC_{ox}\left[V_{GS} - V_{FB} - 2_{\phi F} - \frac{V_{DS}}{2}\right] + \frac{\alpha_x V_{DS}^2}{12\left(V_{GS} - V_T - \frac{\alpha_x}{2} V_{DS}\right)} \tag{250}$$

$$Q_B = WLC_{ox}\left[V_{FB} + 2Q_F - V_T + \frac{(1-\alpha_x)}{2} V_{DS} - \frac{(1-\alpha_x)\alpha_x V_{DS}^2}{12\left(V_{GS} - V_T - \alpha_x \frac{V_{DS}}{2}\right)}\right] \tag{251}$$

$$Q_C = -WLC_{ox}\left[V_{GS} - V_T - \frac{\alpha_x V_{DS}}{2} + \frac{\alpha_x^2 V_{DS}^2}{12\left(V_{GS} - V_T - \alpha_x \frac{V_{DS}}{2}\right)}\right] \tag{252}$$

2. Saturation Region $V_T \le V_{GS} < V_{GSAT}$

$$Q_G = WLC_{ox}\left[V_{GS} - V_{FB} - 2\phi_F - \frac{(V_{GS} - V_T)}{3\alpha_x}\right] \tag{253}$$

$$Q_B = WLC_{ox}\left[V_{FB} + 2\phi_F - V_T + \frac{(1-\alpha_x)(V_{GS} - V_T)}{3\alpha_x}\right] \tag{254}$$

$$Q_C = -WLC_{ox}\left[\frac{2}{3}(V_{GS} - V_T)\right] \tag{255}$$

3. Subthreshold Region $V_{FB} + V_{BS} \le V_{GS} < V_T$

$$Q_G = WLC_{ox}\frac{BE^2}{2}\left[-1 + \sqrt{1 + \frac{4(V_{GS} - V_{FB} - V_{BS})}{BE^2}}\right] \tag{256}$$

$$Q_B = -Q_G \tag{257}$$

$$Q_C = 0 \tag{258}$$

4. Accumulation Region $V_{GS} < V_{FB} + V_{BS}$

$$Q_G = WLC_{ox}(V_{GS} - V_{FB} - V_{BS}) \tag{259}$$

$$Q_B = -Q_G \tag{260}$$

$$Q_C = 0 \tag{261}$$

The mobile channel charge Q_C is partitioned into the drain and source charges, Q_D and Q_S, by considering the following self-consistent boundary conditions:

In the saturation region, the channel is isolated from the drain, so $Q_S = Q_C$ and $Q_D = 0$.

The charges Q_D and Q_S are continuous from the saturation region through the linear region.

The capacitances C_{DG} and C_{SG} are equal, and the charges Q_D and Q_S are equal when V_{DS} is 0.

The capacitances C_{DG}, C_{DS}, C_{DB}, C_{SG}, C_{SD}, and C_{SB} are continuous from the saturation region through the linear region.

According to the above boundary conditions, Q_D and Q_S are given for the saturation region by

$$\begin{aligned} Q_D &= 0 \\ Q_S &= -WLC_{ox}\left[\frac{2}{3}(V_{GS} - V_T)\right] \end{aligned} \tag{262}$$

and for the linear region by

$$Q_D = -WLC_{ox}\left[\frac{V_{GS} - V_T}{2} - \frac{3\alpha_x V_{DS}}{4} + \frac{\alpha_x^2 V_{DS}^2}{8\left(V_{GS} - V_T - \alpha_x \frac{V_{DS}}{2}\right)}\right] \tag{263}$$

$$Q_S = -WLC_{ox}\left[\frac{V_{GS} - V_T}{2} + \frac{\alpha_x V_{DS}}{4} - \frac{\alpha_x^2 V_{DS}^2}{24\left(V_{GS} - V_T - \alpha_x \frac{V_{DS}}{2}\right)}\right] \tag{264}$$

These charge equations have been implemented in SPICE2 to verify that eliminating the calculation of charge from capacitance will result in charge conservation.

G. IMPLEMENTATION OF CHARGE MODEL IN SPICE2 WITH RESULTS

In SPICE2 the error tolerance conditions are specified by

$$V_n^{k+1} - V_n^k \leq E_a + E_r \cdot \max\left(V_n^{k+1}, V_n^k\right) \tag{265}$$

where n is the circuit node number and E_a, E_r are the absolute and relative error tolerances, respectively. For the capacitor in Figure 93, the node voltages will be checked for error tolerance using Equation (265). However, the terminal voltages $(V_1 - V_2)$ and the charge Q_{12} will not be checked for error tolerance compliance in SPICE2. Even though the changes in node voltages V_1 and V_2 may be within the iteration error tolerances, it is possible for $(V_1 - V_2)$ or Q_{12} to be large, in percentage, resulting in nonconservation of charge. This problem was eliminated by implementing the checking of terminal voltages and charge for error tolerance compliance.

The charge model was implemented in SPICE2 and extensively tested against static and dynamic MOSFET circuits including SRAMs, DRAMs, switched capacitor filters, and other MOS VLSI circuits. Figure 94(a) shows a simple charge pumping circuit, which illustrates the usefulness of this new model. This charge pumping circuit presents a severe test for charge conservation. In this circuit, three voltages (V_{gs}, V_{ds}, and V_{bs}) are varying and they switch at different times [Figure 94(b)], so the MOSFET goes through different regions by different paths. If the state variable charge is path dependent, then charge nonconservation will be observed. The simulated output using Meyer's model is shown in Figure 94(c). As a result of nonconservation, the output voltage changes from one cycle to the other cycle no matter how small the tolerances and time steps are. Figure 94(d) shows the simulated output using the new

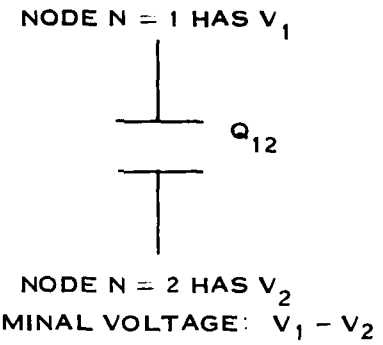


Figure 93. Schematic of Capacitor Nodes, Voltages, and Charge

model. With appropriate tolerances and time steps, the output voltage remains at the correct level from one cycle to the other. This shows that the new model conserves charge. Also, Figure 94(d) shows that with loose tolerances, the output voltage still has small changes from one cycle to another. However, these small changes of output voltage are much smaller than the change of output voltage with Meyer's model and tight tolerances. That is, with this new charge model, the simulation time can be reduced while maintaining better accuracy. Figure 95(a) is the circuit of a switched capacitor low-pass filter. The two clocks ϕ_A and ϕ_B are given in Figure 95(b). The simulated output using Meyer's model is shown in Figure 95(c). According to Meyer's model, the output V_6 has reached steady state. However, the waveform of V_3 indicates that there is a large charge transfer between nodes 1 and 3; that is, V_6 cannot be in steady state. The results are conflicting and nonphysical, and the cause is charge nonconservation. Figure 95(d) shows the simulated output using the new charge model. The waveforms of V_3 and V_6 are consistent and the charge transfers in phases ϕ_A and ϕ_B are equal. Moreover, V_6 rises with the correct time constant as predicted by switched capacitor theory.

Also, with this new charge model, we have an explicit expression for the charge, so the estimates of the truncation errors can be made more accurate. This helps to reduce simulation time even further.

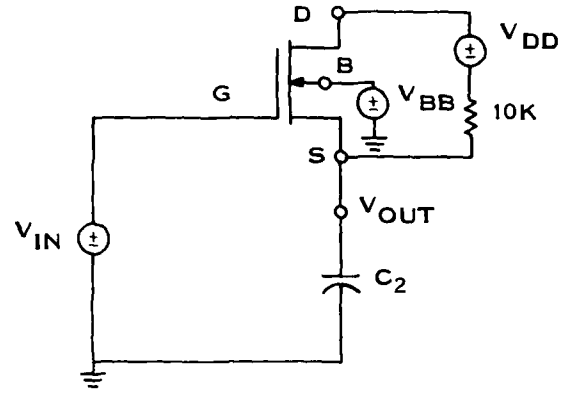
Several static and dynamic MOSFET circuits were analyzed with this new charge model. The size of the circuits ranges from 1 to 1515 transistors. In addition to the increased accuracy, the circuit simulation time is reduced by 18 to 85 percent compared to Meyer's model. The results are given in Tables 9 and 10. Notice that the number of dc iterations is reduced because a better initial guess was implemented.

TABLE 9. SPICE2 MEYER'S CHARGE MODEL COMPARISON

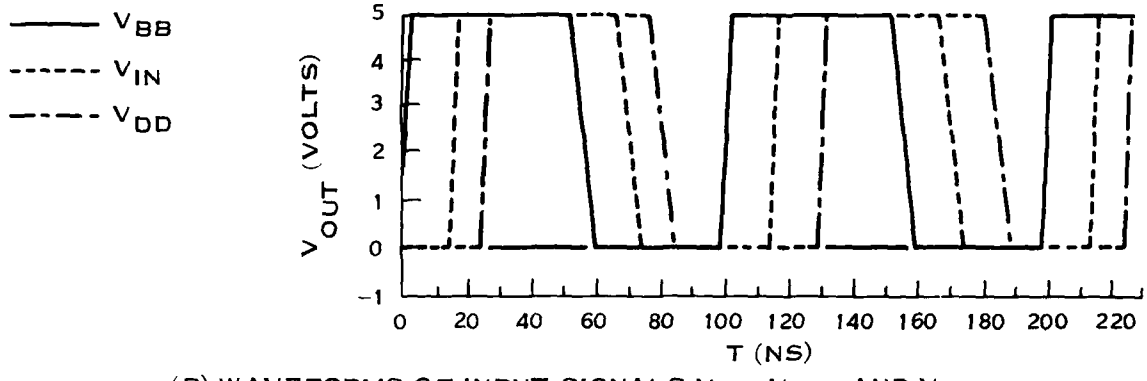
Circuit	1	2	3	4	5	6
Number of dc iterations	18 (10)	14 (6)	28 (27)	36 (24)	26 (17)	68 (49)
CPU time for transient	12.0	47.4	74.7	659.4	56.0	638.1
Analysis in seconds	(8.5)	(6.7)	(60.7)	(405.0)	(40.2)	(357.1)
Percent reduction	29	85	18	38	28	44
Number of MOSFETs	6	1	13	145	6	250

TABLE 10. SPICE2 FIXED/CHARGE MODEL WITH FIXED AND VARIABLE GATE COMPARISON

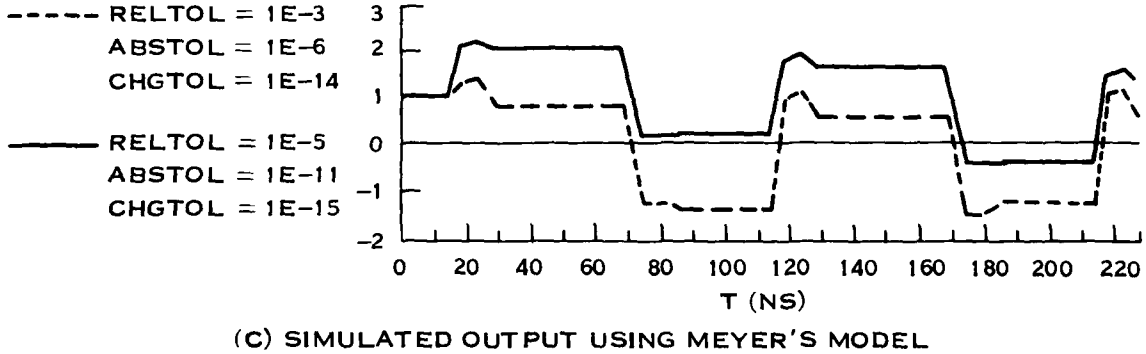
Circuit: 64K dRAM			
Number of dc iterations	29	15	15
CPU time for transient analysis (in seconds)	19,393	16,666	14,372
Percent reduction		15	25
Number of MOSFETs	1515	1515	1515
Intrinsic capacitance model	Fix	Charge	Charge F



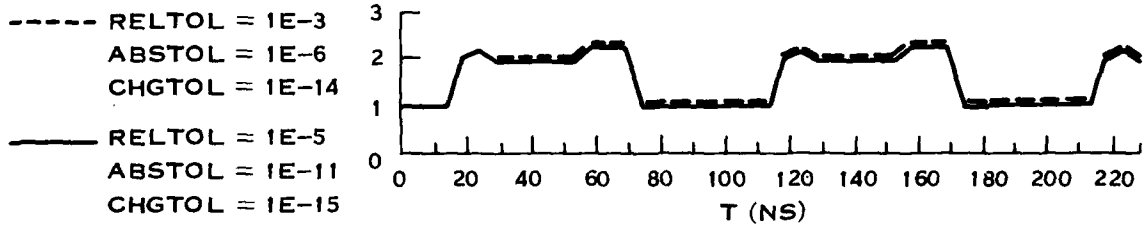
(A) TEST CIRCUIT OF MOSFET AND LINEAR CAPACITORS



(B) WAVEFORMS OF INPUT SIGNALS V_{IN}, V_{BB}, AND V_{DD}

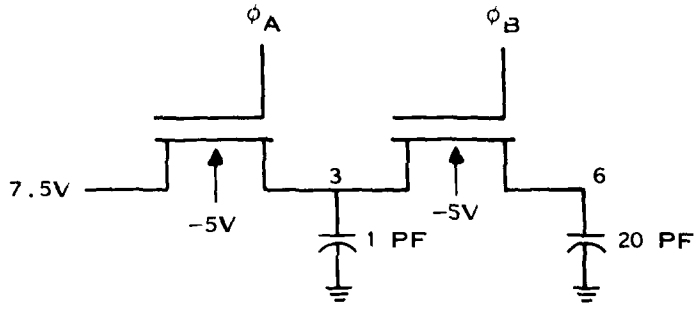


(C) SIMULATED OUTPUT USING MEYER'S MODEL

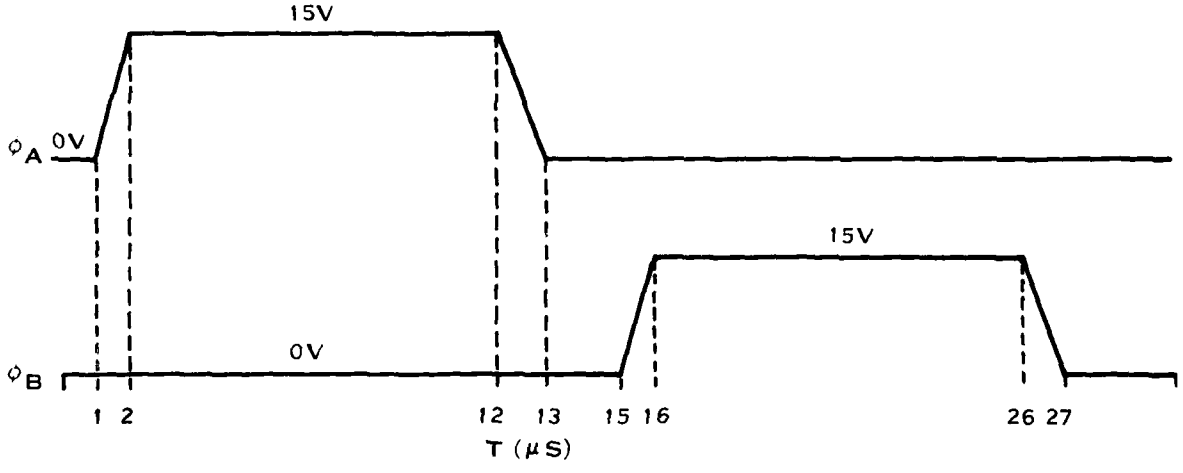


(D) SIMULATED OUTPUT USING NEW CHARGE MODEL

Figure 94. MOSFET and Linear Capacitor Test Circuit, Waveforms, and Simulated Outputs



(A) SWITCHED CAPACITOR LOW-PASS FILTER CIRCUIT



(B) WAVEFORMS OF CLOCKS ϕ_A AND ϕ_B

Figure 95. Switched Capacitor Low-Pass Filter Circuit, Waveforms, and Simulated Outputs (Sheet 1 of 3)

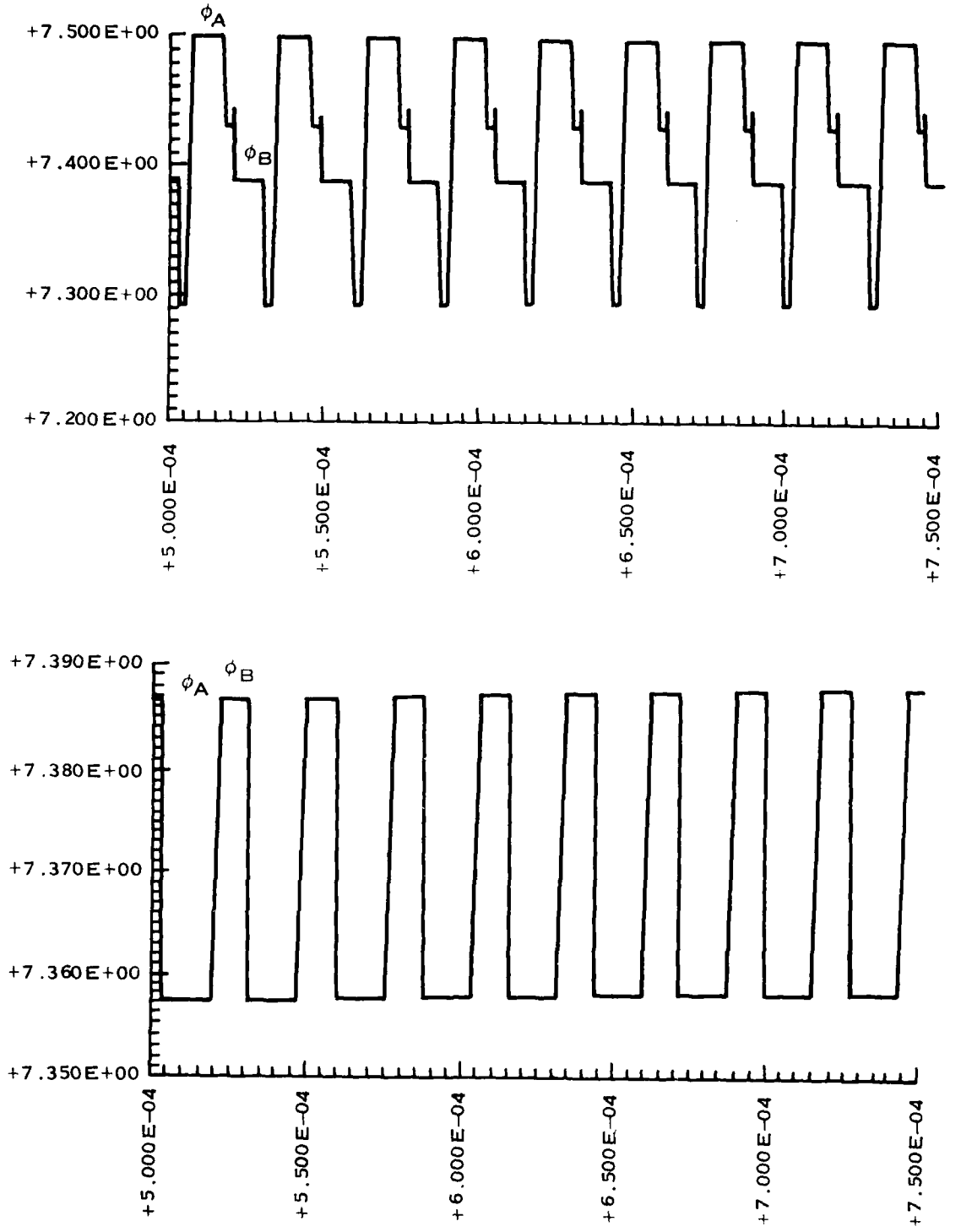


Figure 95. Switched Capacitor Low-Pass Filter Circuit, Waveforms, and Simulated Outputs (Sheet 2 of 3)

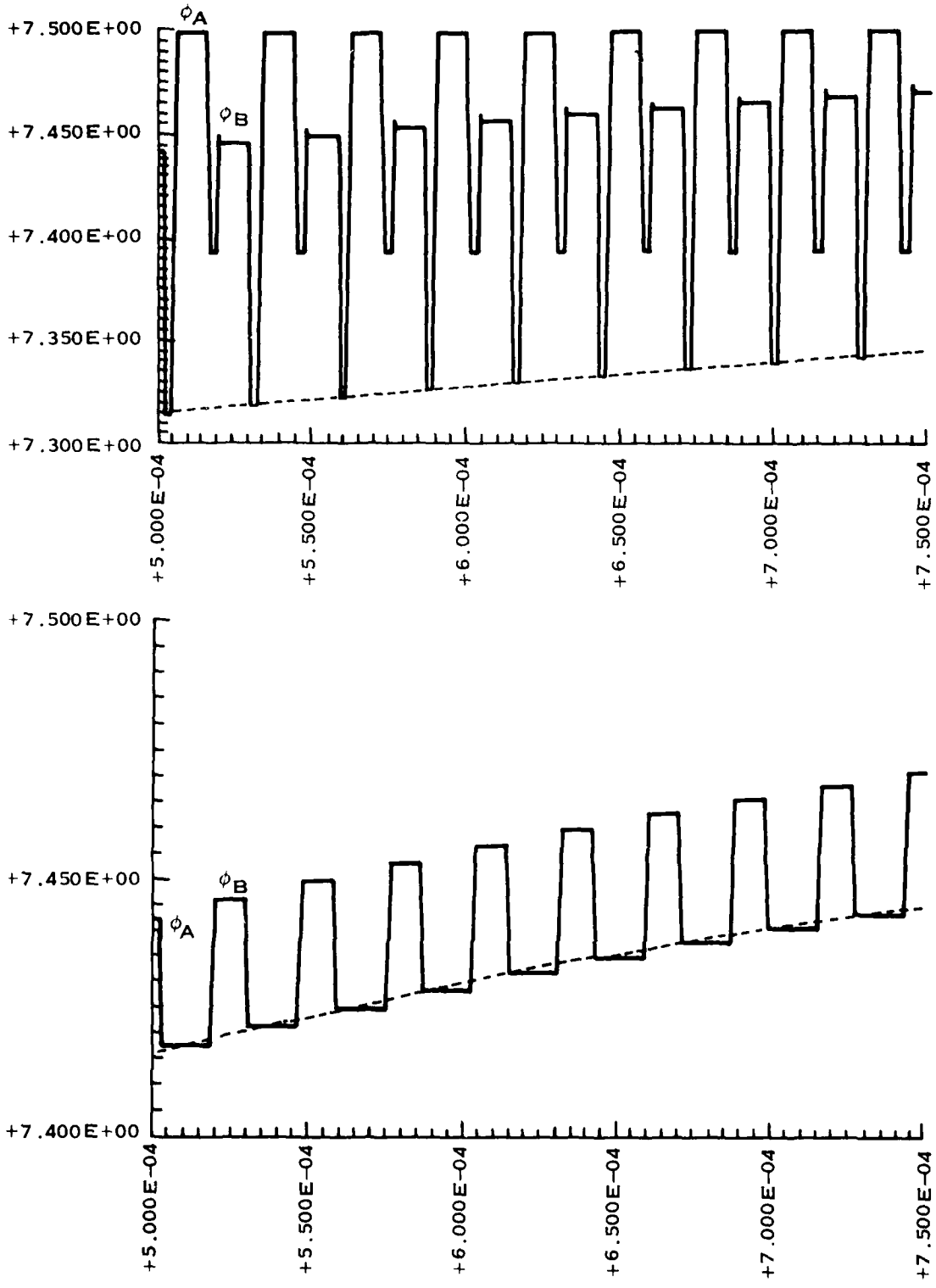


Figure 95. Switched Capacitor Low-Pass Filter Circuit, Waveforms, and Simulated Outputs (Sheet 3 of 3)

SECTION XI

AN OPTIMAL PARAMETER EXTRACTION PROGRAM FOR MOSFET MODELS

A. INTRODUCTION

The accuracy of circuit simulation depends on the accuracy of the device models. For the device model equations to represent the measured I-V characteristic closely, the extraction of model parameter values is required. There are two ways to extract the model parameter values. One way is to perform many special measurements; each measurement is designed to extract one or a few parameter values. This approach is tedious and time-consuming, and because each parameter value is determined by very few data points, the results are not accurate over the entire I-V data space. The other approach is to set up a data acquisition/characterization system, which uses a desk-top or minicomputer to control the measuring instruments and does the necessary analysis to extract the model parameter values. Because this system is completely automated and only the simple measurement of I-V data is performed, this approach is efficient. Also because hundreds of data points are used to represent the entire I-V space, the extracted values of the model parameters are more accurate. For VLSI applications, the second approach is the only feasible choice.

The heart of this parameter extraction system is a nonlinear least-square optimizer, which curve-fits the measured I-V data points to extract the model parameter values. The model equations are put in a separate subroutine that is independent of the optimizer. When the technology or the model is changed, only the model subroutine needs to be updated or modified. This property makes the characterization system extremely flexible. The system will be dealing with hundreds of devices daily and hundreds of I-V data points will be taken for each device, so the optimizer must be reliable and efficient. A proper error function has to be defined and an initial guess algorithm has to be developed to provide a set of good initial values for the model parameters.

The error function is a sum of squares of nonlinear functions, so the general-purpose optimization methods will not provide the best results. Special methods for nonlinear least-square problems have to be used. Nonconvergence is a usual problem for nonlinear optimization algorithms, which is not acceptable for an automated data acquisition/characterization system. An optimization algorithm that guarantees convergence should be used as a backup in the optimizer. In case the regular optimization algorithm fails, this backup algorithm will be used to carry out the parameter extraction.

The optimal parameter extraction program is also useful for the development and the evaluation of new models. If the new model does not have the right dependence, either the fit error will be large or the values of the model parameters will be nonphysical. With the model subroutine independent of the optimizer, different model equations can be tested against measured data with ease.

This optimal parameter extraction program is written in Fortran. The program is extremely efficient; usually it only takes 8 or 9 iterations to converge to the final results. The program size is small, other than the possible restriction of the number of data points allowed, it can be implemented on any desk-top or minicomputer. Those properties make it an extremely useful tool for any frontend.

B. ERROR FUNCTION AND INITIAL GUESS

Let P_i denote the ith unknown model parameter, I_j^M the jth measured current, and $I_j(P_i)$ the jth calculated current obtained from the model equations. The error function we use is

$$ERR = \sum_{\forall I_j^M \geq I_{min}} \left(\frac{I_j - I_j^M}{I_j^M} \right)^2 \tag{266}$$

where I_{min} defines the smallest measured current that will be used for the parameter extraction. The use of I_{min} serves two purposes. One is to exclude bad data points (e.g., the current is smaller than the leakage current or is smaller than the precision of the measuring instruments); the other is to avoid dividing by zero. The advantage of this error function is that it provides a percentage error and does not give too much emphasis either on low currents or on high currents.

To provide a proper set of initial guesses, the following simplified MOSFET current equation[81] is used to choose the most significant parameters to initiate the optimization process.

$$I_D = \begin{cases} \beta_{no}(V_{GS} - V_T)^2 & V_{GS} \geq V_T + V_{DS} \\ \beta_{no}[2(V_{GS} - V_T)\, V_{DS} - V_{DS}^2] & V_T + V_{DS} \geq V_{GS} \geq V_T \\ 0 & V_T > V_{GS} \end{cases} \tag{267}$$

$$V_T = V_{TO} + BE(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}) \tag{268}$$

These simplified equations are used to fit a selected subset of the current data points. It is much easier to extract the values of V_{TO} and β_{no} from the linear region data. This subset is selected by the following criteria to make sure that most of the data points will be in the linear region. Let V_{min} be the smallest V_{DS} that is greater than 0.1 V. The selected data point has a V_{GS} greater than V_{min} and a V_{DS} equal to V_{min}.

With this approach, we can obtain a reasonable set of initial values for β_{no}, V_{TO} and BE.

C. OPTIMIZATION METHODS

The objective here is to find a set of parameter values that will minimize the error function ERR. There are two classes of gradient methods for optimization: the Newton (or quasi-Newton) methods and the modified Gauss methods. The most widely used general-purpose optimization method is the Davidon-Fletcher-Powell (DFP) algorithm,[82] which belongs to the class of quasi-Newton methods. For the MOSFET model parameter extraction, however, the DFP algorithm is not the proper choice. The error function ERR is a sum of squares of nonlinear functions, and the MOSFET model parameter extraction is a nonlinear least square fit problem. It has been reported that the modified Gauss method[83,84] is the best for this class of problems and converges faster than the general-purpose DFP method.[85] Also for the error function ERR, the modified Gauss method is superior to the quasi-Newton method. This can be explained by the following example. Consider the case when there is only one datum point. If the quasi-Newton method is used, we need to find a V^*_{TO} for which

[81]W.N. Carr and J.P. Mize, *MOS/LSI Design and Application*, McGraw-Hill (New York, 1972).

[82]R. Fletcher and M.J.D. Powell, "A Rapidly Convergent Descent Method for Minimization," *The Computer Journal*, **6** (1963), pp. 163–168.

[83]K. Levenberg, "A Method for the Solution of Certain Nonlinear Problems in Least Squares," *Quart. Appl. Maths.*, **2** (1944), pp. 164–168.

[84]D.W. Marquardt, "An Algorithm for Least-Squares Estimation of Nonlinear Parameters," *J. Soc. Indust. Appl. Maths.*, **11** (1963), pp. 431–441.

[85]Y. Bard, "Comparison of Gradient Methods for the Solution of Nonlinear Parameter Estimation Problems," *SIAM Journal on Numerical Analysis*, 7 (1970), pp. 157–186.

$$\left.\frac{d\,ERR}{d\,V_{TO}}\right|_{V_{TO}}$$

is 0. The plots of ERR and $(d\,ERR)/(d\,V_{TO})$ as functions of V_{TO} are given in Figure 96(a) and (b). It can be seen that, if the starting point is not proper (such as V^{n}_{TO}), the iteration will converge to a wrong solution. If the modified Gauss method is used, we need to find a V^{*}_{TO} for which $(I_j - I_j^M)/I_j^M$ is 0. The plot of $(I_j - I_j^M)/I_j^M$ is given in Figure 97. It can be seen that even if the starting point is V^{n}_{TO}, the iteration will still converge to the correct solution V^{*}_{TO}.

As discussed above, the modified Gauss methods are the proper choice for the MOSFET model parameter extraction. The basic principle of the modified Gauss method is given below. Let P_i^k be the kth

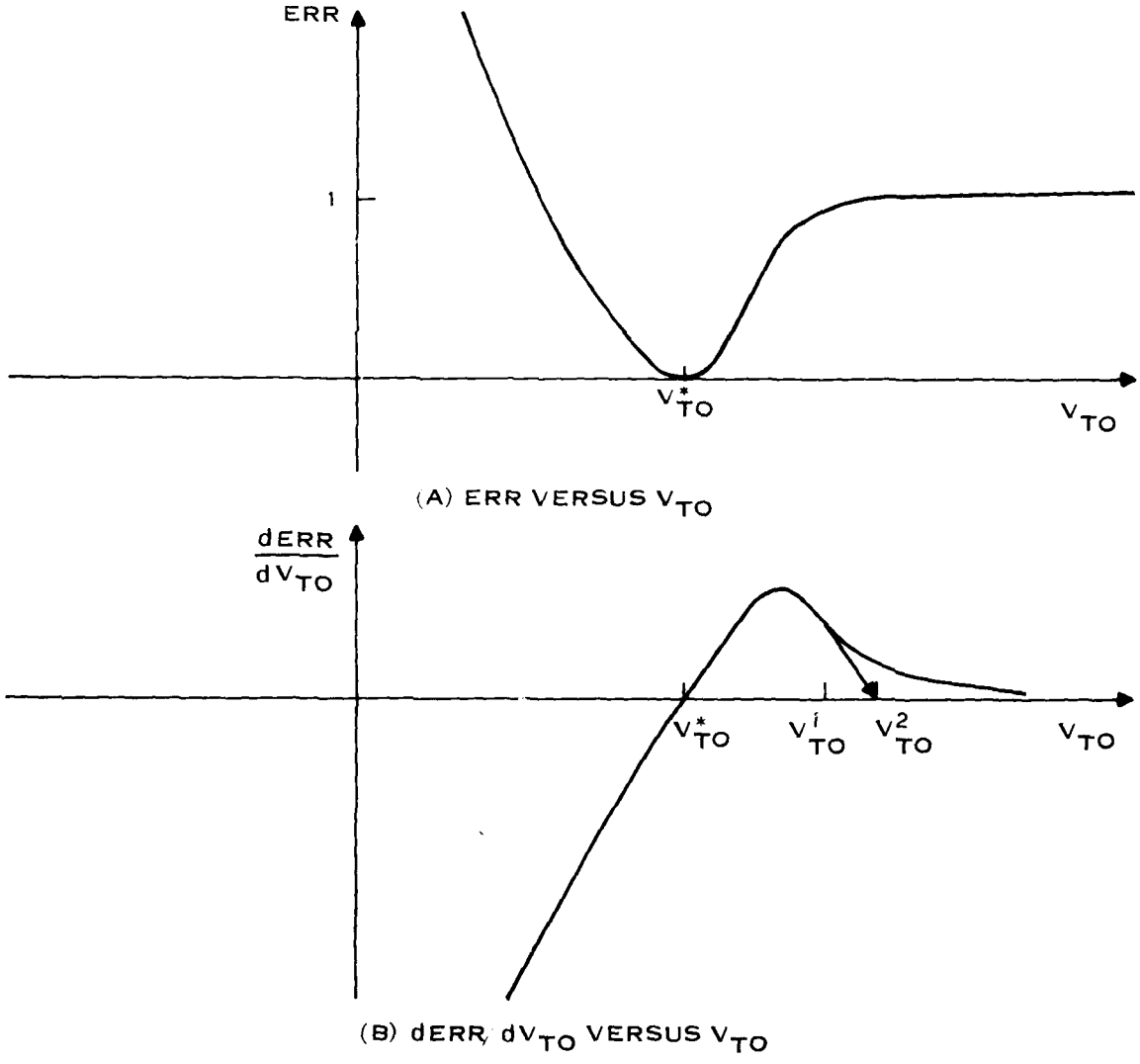


Figure 96. Iteration Convergence to Wrong Solutions for Wrong Starting Points

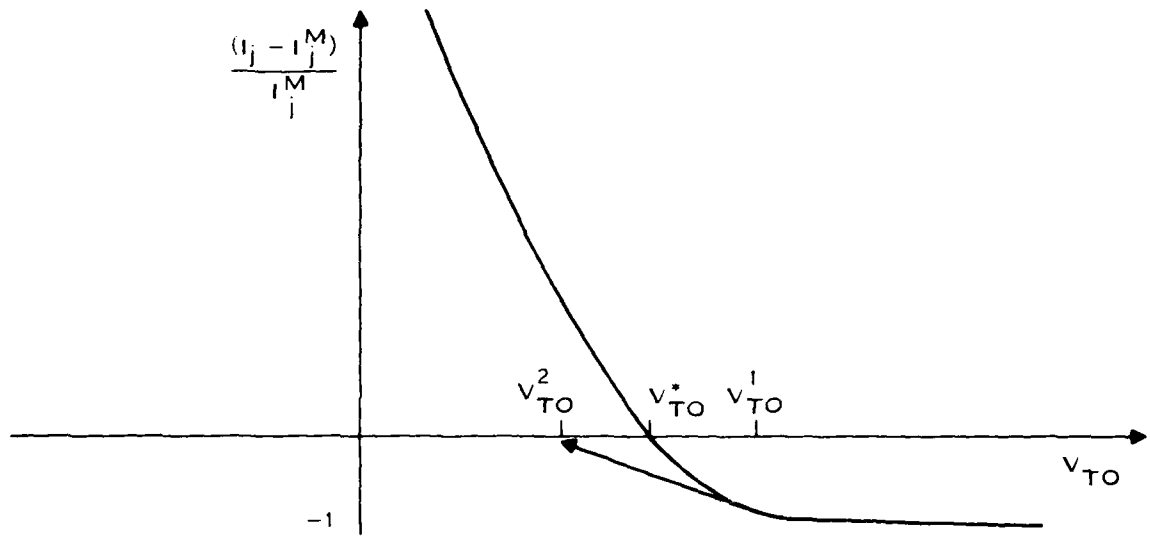


Figure 97. Iteration Convergence to Correct Solution

iteration value for the ith parameter, NP the number of parameters, ND the number of data points, $P^k = (P_1^k, P_2^k, \ldots P_{NP}^k)^T$, and

$$\begin{aligned} Y &= \left[\left(\frac{I_1}{I_1^M}\right)^1, \left(\frac{I_2}{I_2^M}\right)^1, \ldots, \left(\frac{I_{ND}}{I_{ND}^M}\right)^1\right]^T \\ &= (Y_1, Y_2, \ldots, Y_{ND})^T \end{aligned} \tag{269}$$

The error function ERR in Equation (266) can be rewritten as

$$ERR = Y^T Y \tag{270}$$

The basic idea of the modified Gauss method is to find a parameter vector P^* for which Y is approximately 0; that is, we are solving the equation

$$Y \approx 0 \tag{271}$$

Using the Newton-Raphson method, the iteration equation is given by

$$Y_j^{k+1} \approx 0 = Y_j^k + \sum_{i=1}^{Np} \left.\frac{\partial Y_j}{\partial Y_i}\right|_{P_i^k} (P_i^{k+1} - P_i^k) \qquad j = 1, 2, \ldots, ND \tag{272}$$

Equation (272) can be rewritten in the form

$$Y^{k+1} \approx 0 = Y^k + J_{NP}(P^{k+1} - P^k) \tag{273}$$

where

$$J = ND \begin{bmatrix} \frac{\partial Y_1}{\partial P_1} & \frac{\partial Y_1}{\partial P_2} & \cdots & \frac{\partial Y_1}{\partial P_{NP}} \\ \frac{\partial Y_2}{\partial P_1} & \frac{\partial Y_2}{\partial P_2} & \cdots & \frac{\partial Y_2}{\partial P_{NP}} \\ \vdots & \vdots & & \vdots \\ \frac{\partial Y_{ND}}{\partial P_1} & \frac{\partial Y_{ND}}{\partial P_2} & \cdots & \frac{\partial Y_{ND}}{\partial P_{NP}} \end{bmatrix} \tag{274}$$

For the model parameter extraction, the number of data points ND is much larger than the number of parameters NP; that is, Equation (272) describes an overdetermined system.

To obtain P^{k+1}, we can multiply Equation (272) by J^T

$$J^T Y^k + (J^T J)(P^{k+1} - P^k) = 0 \tag{275}$$

Equation (275) can be rewritten as

$$\Delta P^{k+1} = P^{k+1} - P^k = -(J^T J)^{-1} J^T Y^k \tag{276}$$

In general, the P^{k+1} or ΔP^{k+1} obtained from Equation (276) is not the best iterative formula. A superior variant of Equation (276) is

$$\begin{aligned} P^{k+1} &= P^k + \lambda \Delta P^{k+1} \\ &= P^k - \lambda (J^T J)^{-1} J^T Y^k \end{aligned} \tag{277}$$

where λ is usually determined by linear search. For model parameter extraction when the number of data points is much larger than the number of parameters, however, a linear search is time-consuming. An efficient alternative is given as follows. At every iteration, let λ be 1 first. If the error calculated is smaller than the error at the previous iteration, continue to the next iteration; otherwise, λ is divided by 2 and the new error is compared with the error at the previous iteration. This process is repeated until the error is smaller than the error at the previous iteration or λ is smaller than λ_{min}.

The modified Gauss method does not guarantee convergence. This is not acceptable for model parameter extraction. A simple method that guarantees convergence is the steepest descent method. The rate of convergence for the steepest descent method, however, can be slow, so it should not be used as the regular optimization method. Our strategy is to use a combination of both algorithms. The steepest descent method is used as a backup to carry out the extraction of model parameters when the modified Gauss method fails to converge.

D. IMPLEMENTATION

To use Equation (277) to obtain P^{k+1}, we need to use Equation (274) to calculate $J^T J$ and $J^T Y^k$.

$$J^T J = \begin{bmatrix} \sum_j^{ND}\left(\frac{\partial Y_j}{\partial P_1}\right)^2 & \sum_j^{ND}\left(\frac{\partial Y_j}{\partial P_1}\frac{\partial Y_j}{\partial P_2}\right) & V_T + .V_{DS} \geq V_{GS} \geq V_T \\ \sum_j^{ND}\left(\frac{\partial Y_j}{\partial P_1}\frac{\partial Y_j}{\partial P_2}\right) & \sum_j^{ND}\left(\frac{\partial Y_j}{\partial P_1}\frac{\partial Y_j}{\partial P_2}\right) & \cdots \quad \sum_j^{ND}\left(\frac{\partial Y_j}{\partial P_2}\frac{\partial Y}{\partial P_{NP}}\right) \\ \vdots & \vdots & \vdots \\ \sum_j^{ND}\left(\frac{\partial Y_j}{\partial P_{NP}}\frac{\partial Y_j}{\partial P_1}\right) & \sum_j^{ND}\left(\frac{\partial Y_j}{\partial P_1}\frac{\partial Y_j}{\partial P_2}\right) & \cdots \quad \sum_j^{ND}\left(\frac{\partial Y_j}{\partial P_2}\frac{\partial Y_j}{\partial P_{NP}}\right) \end{bmatrix} \tag{278}$$

$$J^T Y^k = \begin{bmatrix} \sum_j^{ND} \frac{\partial Y_j}{\partial P_1} Y_j^k \\ \sum_j^{ND} \frac{\partial Y_j}{\partial P_2} Y_j^k \\ \vdots \\ \sum_j^{ND} \frac{\partial Y_j}{\partial P_{NP}} Y_j^k \end{bmatrix} \tag{279}$$

As mentioned before, having the optimizer independent of the model equations is desirable, hence, evaluating $\partial Y_j/\partial P_i$ directly is not. Instead, we would like to evaluate $\partial I_j/\partial P_i$ and then calculate $\partial Y_j/\partial P_i$ indirectly. From Equations (266) and (269), we obtain

$$\frac{\partial Y_j}{\partial P_i} = \frac{\frac{\partial I_j}{\partial P_i}}{I_j^M} \tag{280}$$

Because the number of parameters NP is usually small, the CPV time for the matrix inversion of J^TJ is negligible, and thus sparse matrix technique is not used in the program. The use of the full matrix technique gives the program some extra benefits with ease. The initial, minimum, and maximum values of the model parameters are specified in the input file. If the minimum and maximum values of any model parameter equal the initial value, the value of that model parameter will be fixed in the program. This is accomplished by not calculating the particular row and column corresponding to that parameter, in Equations (278) and (279); instead, a unit row and column is used in Equation (280) and a 0 is used in Equation (279). Another benefit is the avoidance of 0 determinant. From Equation (280), if $\partial I_j/\partial P_i$ equals 0, then $\partial Y_j/\partial P_i$ equals 0. When a particular combination of model parameter values $\partial I_j/\partial P_i$ equals 0 for all data points, the row i of J^TJ will be a 0 row and the row i of J^TY^k will be 0. A 0 row makes it impossible to do the matrix inversion. This problem can be easily resolved by setting $(J^TJ)_{ii}$ to be 1.

At every iteration, the error ERR^{k+1} and the $\lambda\Delta P^{k+1}$ are calculated; if one of the following two conditions is satisfied, the process is considered to have converged.

$$|ERR^{k+1} - ERR^{k}| \leq \text{RELTOL}^{*} \max(|ERR^{k+1}|, |ERR^{k}|) + \text{ABSTOL} \tag{281}$$

$$|\lambda\Delta P^{k+1}| \leq \text{RELTOL}^{*} \max(|P^{k+1}|, |P^{k}|) + \text{ABSTOL} \tag{282}$$

where RELTOL and ABSTOL are the relative and absolute error tolerances. Usually, RELTOL = 1E−6 and ABSTOL = 1E−12 is used to guarantee accurate results.

E. DEVICE PROCESS PARAMETER EXTRACTION

This optimizer is not only useful for circuit model parameter extraction but also for device process parameter extraction. For example, a common practice at a process characterization laboratory is to use the linear region I-V data to extract the threshold voltage, the device gain, and the mobility degradation factor. This task can be easily accomplished by using the proper model equations and the linear region I-V data in the optimizer. Another common practice is to extract the width and length reductions for the gains of different devices. This task can also be easily done by using the gains of different devices as the data and using the width and length reduction equations as the model equations.

F. RESULTS AND CONCLUSIONS

This optional parameter extraction program is written in Fortran and is implemented on an HP-1000F minicomputer. The accuracy and efficiency has been verified by routinely using the optimizer for a large variety of MOSFET device parameter extractions. An overlay of the I-V curve computed from the extracted parameters and the measured I-V data for a 5- by 1.5-mm MOSFET is given in Figure 98.

The percentage error, number of iterations, and values of the extracted parameters are given in Table 11. The percentage as defined by Equation (266) for this example is 1.8 percent. Because parameter variation in the process is generally much larger, the accuracy of the extracted parameter vector is deemed to be adequate for circuit analysis. Figure 99 gives a distribution of the number of iterations for a total of 85 different devices.

The total number of data points per device is 628, the relative error RELTOL is 1E−6 and the absolute error ABSTOL is 1E−12. Normally, it only takes about eight iterations for the optimizer to converge. This demonstrates the efficiency of the optimizer.

TABLE 11. EXTRACTED PARAMETER VALUES

FIT ERR = 1.8 Percent
NUMBER OF ITERATIONS = 9

Parameter	Value
β_{no}	0.14723811E−03
V_{FB}	0.97309162E+00
ϕ_f	0.36000000E+00
BE	0.13187124E+00
α	0.94910257E+00
θ	0.33156107E+00
λ	0.10031323E+00
γ	0.14570696E+00
DE	0.11586447E+00

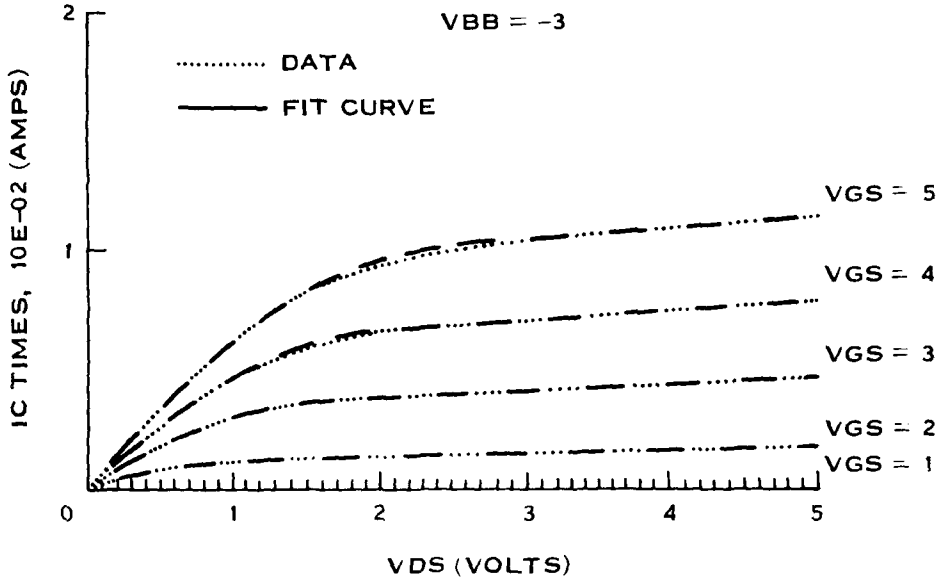


Figure 98. Calculated and Measured I-V Data for a 5- by 1.5-μm MOSFET

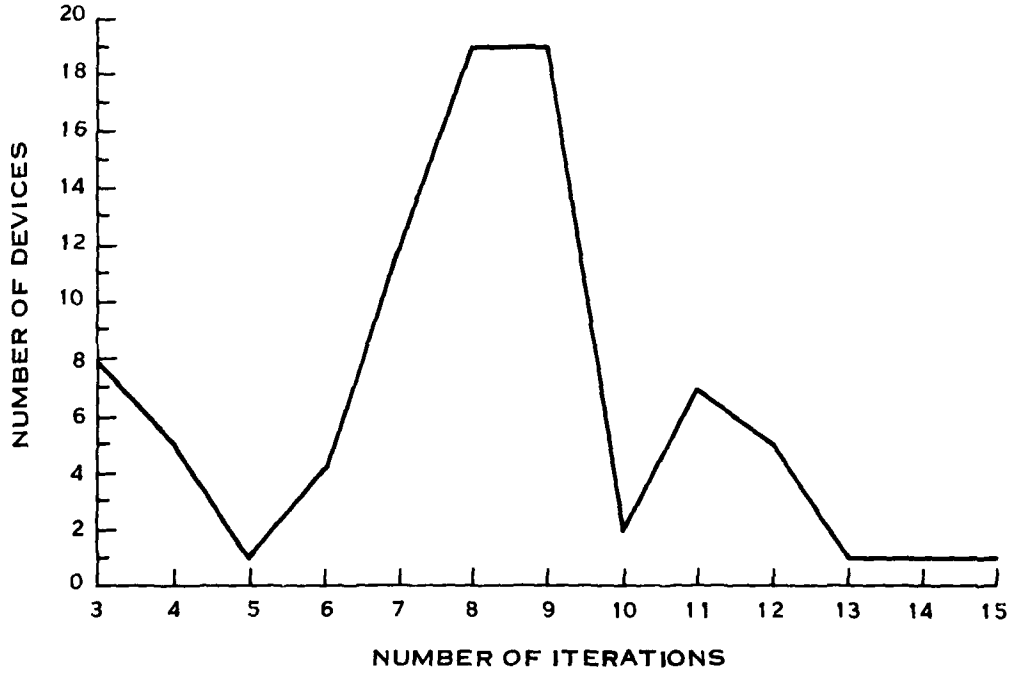


Figure 99. Distribution of Iterations for 85 Devices

SECTION XII

ANALYSIS OF THE 2-DIMENSIONAL DEVICE MODELING PROGRAM GEMINI

Considerable effort has been expended to thoroughly understand the operation of the Stanford University two-dimensional Poisson solver GEMINI. We have found the flexible input capabilities for specifying the device structure and the graphics output of the program to be important features. Problems found with the physics of the program are identified below.

The capability of specifying the source/drain distributions using either a Gaussian or complementary error function distribution was found to be in error. Subroutine DFEVL was rewritten to handle this problem using the following approach. Given the input parameters

DX	Defined in Figure 100
N_D	Implanted dose of ion in source/drain region in cm^{-2}
N_B	Background concentration in cm^{-3}
Y_j	Verticle junction depth of source/drain
RXY	Ratio of the characteristic length in the x direction to that in the y direction (LX/LY)

the horizontal impurity distribution, assuming a complementary error function form, can be found by solving the equation

$$\frac{N_D}{2\sqrt{\pi Ly}} \exp\left[-\left(\frac{Yj}{Ly}\right)^2\right]\left[\operatorname{erfc}\left(\frac{-DX}{2 \cdot Ly \cdot Rxy}\right) - \operatorname{erfc}\left(\frac{DX}{2 \cdot Ly \cdot Rxy}\right)\right] = N_B \tag{283}$$

for Ly using the Newton-Raphson technique. This is done by defining

$$F(Ly) \equiv \frac{N_D}{2\sqrt{\pi}} \exp\left[-\left(\frac{Yj}{Ly}\right)^2\right]\left[\operatorname{erfc}\left(\frac{-DX}{2 \cdot \mathrm{LY} \cdot RXY}\right) - \operatorname{erfc}\left(\frac{DX}{2 \cdot Ly \cdot Rxy}\right)\right] - N_B L_y = 0 \tag{284}$$

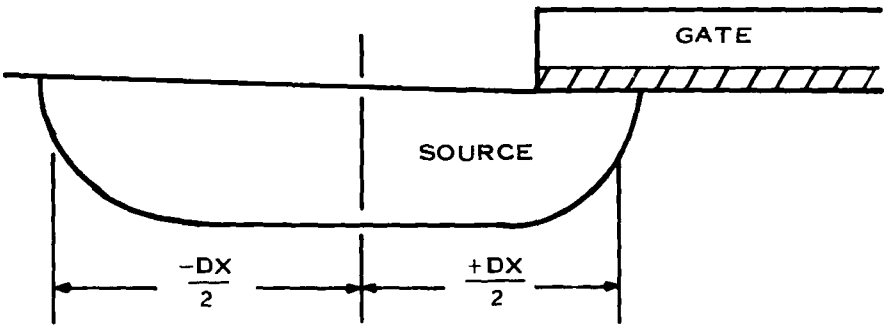


Figure 100. Definition of Source/Drain for Complementary Error Function Distribution

thus

$$Ly(i+1) = Ly(i) - \frac{F[Ly(i)]}{F'[Ly(i)]} \tag{285}$$

If the peak concentration of the distribution is input rather than the total dose, then the relationship

$$N_p = \frac{N_D}{\sqrt{\pi}\, Ly} \tag{286}$$

can be substituted into Equation (284).

If the horizontal impurity distribution is Gaussian, then Equation (284) is replaced by

$$F(Ly) = \frac{\sqrt{\pi}\, N_B\, Ly}{N_D} - \exp\left[-\left(\frac{Yj}{Ly}\right)^2 \right] = 0 \tag{287}$$

The solution of Poisson's equation

$$\nabla \cdot \mathrm{D} = \rho \tag{288}$$

is accomplished by assuming complete ionization of impurities in subroutine NUSET

$$\rho = -q\,(N_D^{+} - N_A^{-}) \tag{289}$$

However, in the source/drain regions the doping levels may exceed the effective density of states N_C or N_V so the complete ionization assumption will result in built-in voltages for the source/drain diodes of 2 to 3 volts. This nonphysical result can be corrected by using the Fermi-Dirac distribution functions and charge neutrality.

$$N_D^{+} = \frac{N_D}{1 + 2\exp\left[q\,(V - V_{fn} + V_D)/\mathrm{k}T\right]} \tag{290}$$

$$N_A^{-} = \frac{N_A}{1 + \tfrac{1}{4}\exp\left[q\,(V_{fp} + V_A - V - V_G)/\mathrm{k}T\right]} \tag{291}$$

$$N_D^{+} - N_A^{-} + p - n = 0 \tag{292}$$

where V_D is the donor voltage level measured with respect to the conduction band edge, V_A is the acceptor voltage level measured with respect to the valence band edge, V_G is the band gap voltage, V is the conduction band voltage, and V_{fp} and V_{fn} are the hole and electron quasi-Fermi levels. These equations can be solved for V by using the Newton-Raphson method where

$$\begin{aligned} \mathrm{F(V)} = {} & \frac{N_D}{1 + 2\exp\left[q\,(V - V_{fn} + V_D)/\mathrm{k}T\right]} - \frac{N_A}{1 + \tfrac{1}{4}\exp\left[q(V_{fp} + V_A - V - V_G)/\mathrm{k}T\right]} \\ & - \frac{2}{\sqrt{\pi}} N_C F_{\nu_2}\left[q\,(V - V_{fn})/\mathrm{k}T\right] + \frac{2}{\sqrt{\pi}} N_V F_{\nu_2}\left[q\,(V_{fp} - V_G - V)/\mathrm{k}T\right] = 0 \end{aligned} \tag{293}$$

thus,

$$V_{i+1} = V_i - \frac{F(V_i)}{F'(V_i)} \tag{294}$$

N_D^+ and N_D^- can be found from Equations (290) and (291).

Because GEMINI only solves Poisson's equation, the drain current is calculated using the expression:

$$I_{DS} = -q\, D_n\, W\, Q_B\, [-qV_{DS}/\mathrm{k}T)] \tag{295}$$

where

$$Q_B = \frac{Z^*}{L^*} \frac{n_i^2}{N_B} \exp\, [q\, (\psi^* - V_S)/\mathrm{k}T] \tag{296}$$

The value of Q_B is computed in subroutine ECHAN; however, the value of V_S is not available in this subroutine. As long as V_S is 0, the correct Q_B is calculated; however, V_S must be brought into the subroutine to correctly calculate Q_B when V_S is not 0.

We have found that the coordinates of the potential extremum determined by GEMINI depend on the values of x·min, x·max, y·min, and y·max. If the potential extremum is found for a given solution using x·min1, x·max1, y·min1, y·max1 as the search region and then a new search region y·min2, x·max2, y·min2, y·max2 is defined that encloses the previously found potential extremum, a new potential extremum value will be found rather than the original one. An example is included to illustrate the problem. Figure 101 defines the device while Figure 102 gives one potential extremum while Figure 103 gives another. We have not located the cause of this problem.

Since GEMINI does not solve the current continuity equation, the assignment of the quasi-Fermi levels is made in an arbitrary manner as shown in Figure 104. Because of the location of E_{fn}-channel with respect to E_C-channel, the calculation of the electron concentration in the channel will be many orders of magnitude in error as will the current that is computed from it. We intend to modify the assignment of these quasi-Fermi levels including adding gradient in the channel region to more accurately represent a real device.

```
COMMENT     Example 1—NMOS channel length simulation
COMMENT     Device structure definition

STRUCTURE   TEMPERATURE=300  DATA.OUT=WA1STR VOL.RATI=0.0

COMMENT     Define the device solution region
SUBSTRATE   CONCENTRATION=1.25E15 P-TYPE  WIDTH=5.0  DEPTH=3

COMMENT     Define the discretization grid
GRID        XGRD.MIN=.01  XGRD.MAX=.15  X.SPACES=50
+           YGRD.MIN=.01  Y.SPACES=50

COMMENT     Define the insulator regions
INSULATOR   SOURCE THICKNESS=.100  WIDTH=1.30  ENCROACH=.9
INSULATOR   GATE THICKNESS=.550
INSULATOR   DRAIN THICKNESS=.100  WIDTH=1.30  ENCROACH=.9

COMMENT     Define the top surface electrodes
ELECTRODE   GATE N-POLY WIDTH=4.8  LEFTEDGE=0.1

COMMENT     Define the top interface charge
QSS         CONCENTRATION=5.E10

COMMENT     Define the channel enhancement implant
PROFILE     CHANNEL  IMPLANT  P-TYPE  PEAKCONC=1.530E16
+           Y.PEAK=0.14  Y.CHAR=0.300
PROFILE     CHANNEL  IMPLANT  P-TYPE  PEAKCONC=0.350E16
-           Y.PEAK=0.00  Y.CHAR=0.024
COMMENT     Define the source and drain diffusions
PROFILE     SOURCE DIFFUSION  N-TYPE  PEAKCONC=1.00E22
+           Y.CHAR=0.1300  WIDTH=1.00        XY.RATIO=0.65
PROFILE     DRAIN  DIFFUSION  N-TYPE  PEAKCONC=1.00E22
+           Y.CHAR=0.1300  WIDTHI=1.00       XY.RATIO=0.65
FND         Structure definition

COMMENT     Example 1—NMOS channel length simulation
COMMENT     Poisson Solution Definition

COMMENT     Define the device structure with EXISTR
STRUCTURE   DATA INP=WA1STR

COMMENT     Perform the solution of Poisson's equation
SOLUTION    DATA OUT=WA1SOL::-14  W.N+POLY=4.17

COMMENT     Define the bias voltages
COMMENT     VB=0.0,  VS=0.0, VD=0.0, VG=5.0
BIAS        GATE POTENTIAL=0.0
BIAS        SUBSTRATE POTENTIAL=0.000
BIAS        SOURCE POTENTIAL=0.0
BIAS        DRAIN POTENTIAL=30.00
END         Solution definition
```

Figure 101. Definition of Device to Illustrate Dependence of Potential Extremum on Search Region

```
****************************************
***          GEMINI-I                ***
***     VERSION 1A REV. 8029         ***
****************************************
```

Commands input from file WA1PC

```
1...  COMMENT   One-dimensional plot of the potential along
2...  +         the current channel path

3...  PLOT.1D   POTENTIAL  LEFT=0          RIGHT=5.0
      +                    BOTTOM=0.0     TOP=5.00

4...  MAXIMUM   X.MIN=0  X.MAX=5.0  Y.MIN=0.0  Y.MAX=0.800  ←
      +         DATA.INP=WA1SOL

5...  END
```

One-dimensional plot of the potential along the current channel path

Extreme potential = 1.291E−01 volts ←
Impurity concentration = 1.409E+15 #/cm**3
Minority carrier concentration = 2.616E+07 #/cm**3
At X = 1.510E+00 microns
Y = 7.809E−01 microns ←

Left pi*kT/4q point = 1.485E+00 microns
Right pi*kT/4q point = 1.547E+00 microns
Effective length = 7.234E−02 microns
Effective width = 6.159E−02 microns
Width/length ratio = 8.514E−01
Barrier charge concentration QB = 2.227E+07 #/cm**3
Total charge concentration QW = 3.694E+11 #/cm
Conductive charge concentration QL = 4.043E-27 #/cm**3
Barrier loss factor = 4.602E+07 #/cm**2

*** END GEMINI ***

Figure 102. First Search Region to Illustrate Dependence of Extreme Potential on Search Region

```
*****************************************
***          GEMINI-I                 ***
***     VERSION 1A REV. 8029          ***
*****************************************
```

Commands input from file WA1PC

```
1...  COMMENT   One-dimensional plot of the potential along
2...  +         the current channel path

3...  PLOT.1D   POTENTIAL  LEFT=0          RIGHT=5.0
      +                    BOTTOM=0.0     TOP=5.00

4...  MAXIMUM   X.MIN=0  X.MAX=5.0  Y.MIN=0.0  Y.MAX=1.000  ←
      +         DATA.INP=WA1SOL

5...  END
```

One-dimensional plot of the potential along the current channel path

```
Extreme potential = 1.785E-01 volts  ←
Impurity concentration = 4.536E+16 #/cm**3
Minority carrier concentration = 1.765E+08 #/cm**3
  At X = 1.450E+00 microns
  Y = -2.274E-08 microns  ←

Left pi*kT/4q point = 1.441E+00 microns
Right pi*kT/4q point = 1.515E+00 microns
Effective length = 7.198E-02 microns
Effective width = 6.370E-02 microns
Width/length ratio = 8.850E-01
Barrier charge concentration QB = 1.562E+08 #/cm**3
Total charge concentration QW = 3.694E+11 #/cm
Conductive charge concentration QL = 4.043E-27 #/cm**3
Barrier loss factor = 4.602E+07 #/cm**2

*** END GEMINI ***
```

Figure 103. Second Search Region to Illustrate Dependence of Extreme Potential on Search Region

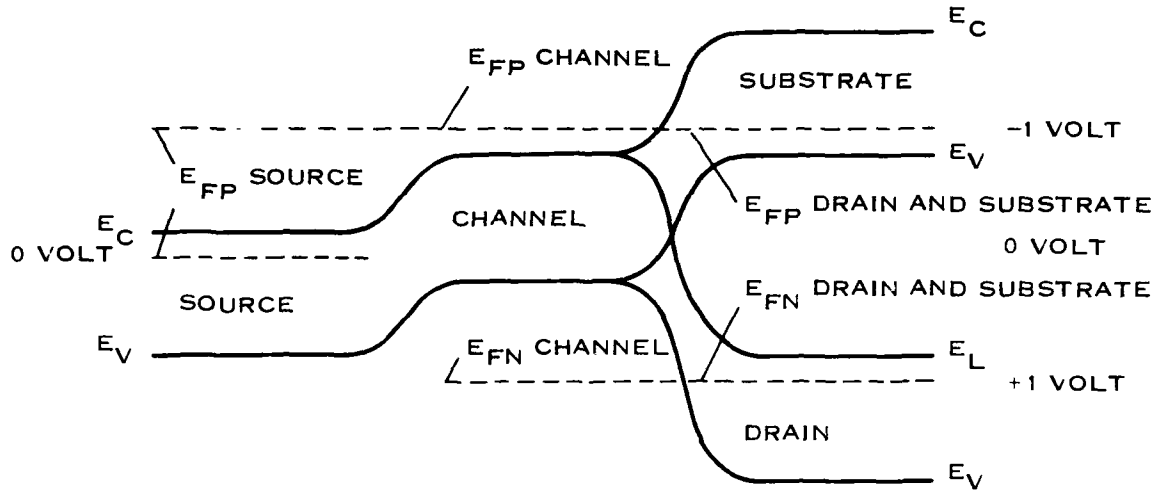


Figure 104. Quasi-Fermi Level Assignment in GEMINI for a MOSFET With $V_G = 0$, $V_D = +1$, and $V_X = -1$

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APPENDIX A

STEP PROFILE APPROXIMATION OF SUBSTRATE DOPING

Because of its analytical facility, step profile approximation is widely used as a replacement for implanted channel doping. Generally, a graphical fit is made and as such the approximated result is often arbitrary. This appendix develops pertinent equations that allow a faithful analytical reduction of the Gaussian implant distributions.

The premise underlying this approach is that for the purpose of device modeling, the fundamental urgency is that the surface electric field as a function of surface potential be preserved. In view of this requisite, the surface electric field as a function of surface potential is calculated for the exact substrate doping distribution as well as a chosen step profile approximation. With a few trials, such a step profile can be generated as would preserve the surface electric field as a function of surface potential within a certain accuracy.

Poisson's equation for the implanted substrate can be written as

$$\frac{d^2\phi}{dx^2} = \frac{q}{\epsilon_s}\left[N_A + \frac{Q_1}{\sqrt{2\pi}S_1}\exp\left\{-\left(\frac{x-R_1}{\sqrt{2}S_1}\right)^2\right\} + \frac{Q_2}{\sqrt{2\pi}S_2}\exp\left\{-\left(\frac{x-R_2}{\sqrt{2}S_2}\right)^2\right\}\right] \tag{A-1}$$

where N_A is the background doping and Q_i, R_i, S_i are the implanted dose, the projected range, and the range straggle for the ith implant respectively.

The surface electric field and surface potential can be found from the solution of (Aq) as

$$E_s = \frac{qN_Ax_D}{\epsilon_s} + \frac{qQ_1}{2\epsilon_s}\left\{\text{erf}\left(\frac{x_D-R_1}{\sqrt{2}S_1}\right) - \text{erf}\left(\frac{-R_1}{\sqrt{2}S_1}\right)\right\} + \frac{qQ_2}{2\epsilon_s}\left\{\text{erf}\left(\frac{x_D-R_2}{\sqrt{2}S_2}\right) - \text{erf}\left(\frac{-R_2}{\sqrt{2}S_2}\right)\right\} \tag{A-2}$$

$$\begin{aligned}\phi_s = {} & \frac{qN_Ax_D^2}{2\epsilon_s} + \frac{qQ_1R_1}{2\epsilon_s}\left\{\text{erf}\left(\frac{x_D-R_1}{\sqrt{2}S_1}\right) - \text{erf}\left(\frac{-R_1}{\sqrt{2}S_1}\right)\right\} - \frac{qQ_1S_1}{\sqrt{2\pi}\epsilon_s}\left\{\exp-\left(\frac{x_D-R_1}{\sqrt{2}S_1}\right)^2\right. \\ & \left. - \exp-\left(\frac{R_1}{\sqrt{2}S_1}\right)^2\right\} + \frac{qQ_2R_2}{2\epsilon_s}\left\{\text{erf}\left(\frac{x_D-R_2}{\sqrt{2}S_2}\right) - \text{erf}\left(\frac{-R_2}{\sqrt{2}S_2}\right)\right\} \\ & - \frac{qQ_2S_2}{\sqrt{2\pi}\epsilon_s}\left\{\exp-\left(\frac{x_D-R_2}{\sqrt{2}S_2}\right)^2 - \exp-\left(\frac{R_2}{\sqrt{2}S_2}\right)^2\right\}\end{aligned} \tag{A-3}$$

A similar treatment of the step approximation gives for

$$x_D \leq t_1$$

$$E_s = \frac{qN_{A1}x_D}{\epsilon_s} \tag{A-4}$$

$$\phi_s = \frac{qN_{A1}x_D^2}{2\epsilon_s} \tag{A-5}$$

for

$$x_D > t_1$$

$$E_s = \frac{qN_{A1}t_1}{\epsilon_s} + \frac{qN_{A2}}{\epsilon_s}(x_D - t_1) \tag{A-6}$$

$$\phi_s = \frac{qN_{A1}t_1^2}{2\epsilon_s} + \frac{qN_{A2}}{2\epsilon_s}(x_D^2 - t_1^2) \tag{A-7}$$

Equations (A2) to (A7) obtain relationship between ϕ_s and E_s with X_D as a parameter. These equations can be used to obtain the exact and the approximated E_s versus ϕ_s plots. The summation of the square of deviation in E_s, from the two plots is calculated as it forms a benchmark in accuracy. Within a few trial step approximations, this error can often be reduced within an acceptable bound.

APPENDIX B

ELECTROSTATICS OF A STEP DOPING PROFILE

When the depletion layer extends in region II, the solution of Poisson's equation yields

$$\left(\frac{d\phi}{dx}\right)_1 = \frac{qN_{A1}}{\epsilon_s}(x - t_1) + \left(\frac{d\phi}{dx}\right)_{2|x=t_1} \tag{B-1}$$

$$\left(\frac{d\phi}{dx}\right)_2 = \frac{qN_{A2}}{\epsilon_s}(x - x_D) \tag{B-2}$$

The surface potential is given by

$$\begin{aligned}\phi_s &= V_X + \int_{x_D}^{t_1}\left(\frac{d\phi}{dx}\right)_2 dx + \int_{t_1}^{0}\left(\frac{d\phi}{dx}\right)_1 dx \\ &= V_X + \frac{qN_{A2}}{2\epsilon_s}(x_D^2 - t_1^2) + \frac{qN_{A1}}{2\epsilon_s}t_1^2\end{aligned} \tag{B-3}$$

which yields

$$X_D = \left\{\frac{2\epsilon_s}{qN_{A2}}\left(\phi_s - V_X - \frac{qN_{A1}t_1^2}{2\epsilon_s}\right) + t_1^2\right\}^{1/2} \tag{B-4}$$

The depletion charge density can be written as

$$\begin{aligned}Q_D &= qN_{A1}t_1 + qN_{A2}(x_D - t_1) \\ &= \{2\epsilon_s qN_{A2}(\phi_s + \phi_A)\}^{1/2} - qt_1(N_{A2} - N_{A1})\end{aligned} \tag{B-5}$$

where

$$\phi_A = \frac{q}{2\epsilon_s}(N_{A2} - N_{A1})t_1^2 - V_X \tag{B-6}$$

APPENDIX C

CALCULATION OF x_i

Using Kirchoff's voltage law and Gauss's law across the back interface

$$V_B = V_X + \frac{qN_{A2}}{2\epsilon_s}(t_s - x_i)^2 + \frac{qN_{A2}}{C_{ob}}(t_s - x_i) + \phi_{BX} - \frac{Q_{f2}}{C_{ob}} + \phi_b \qquad (C-1)$$

where ϕ_b is the voltage drop across the bulk which varies from 0 to $2\phi_{FB}$ in magnitude and may be positive or negative. The exact magnitude and sign can be determined knowing interface charges, applied voltages, doping densities, and buried oxide thickness.

The solution of the quadratic Equation (C-1) yields

$$x_i = t_s + \frac{\epsilon_s}{C_{ob}} - \left\{\left(\frac{\epsilon_s}{C_{ob}}\right)^2 + \frac{2\epsilon_s}{qN_{A2}}\left(V_B - V_X - \phi_{BX} - \phi_b + \frac{Q_{f2}}{C_{ob}}\right)\right\}^{1/2} \qquad (C-2)$$

APPENDIX D

DEVICE THRESHOLD VOLTAGE UNDER SPACE CHARGE INTERACTION

If either the substrate doping or its thickness is small, then the channel depletion layer may start interacting with the back interface depletion region before the device threshold condition is reached. An elemental section of the device along with its charge distribution, electric field variation, and potential profile for such a case is shown in Figure D–1. The edge of the channel depletion layer, x_D, is defined as the location where electric field is 0, as shown in Figure D–1(c).

With the use of Equation (B–3), it follows from Figure D–1(d) that

$$V_G = \phi_{\min} + \frac{qN_{A2}}{2\epsilon_s}(x_D^2 - t_1^2) + \frac{qN_{A1}}{2\epsilon_s}t_1^2 + \frac{1}{C_o}\{qN_{A1}t_1 + qN_{A2}(x_D - t_1)\} + \phi_{GX} - \frac{Q_{f1}}{C_o} \tag{D–1}$$

$$V_B = \phi_{\min} + \frac{qN_{A2}}{2\epsilon_s}(t_s - x_D)^2 + \frac{qN_{A2}}{C_{ob}}(t_s - x_D) + \phi_{BX} - \frac{Q_{f2}}{C_{ob}} + \phi_b \tag{D–2}$$

Elimination of $\phi_{\min}$ from Equations (D–1) and (D–2), and rearrangement yields the edge of the depletion region, which communicates with V_G as

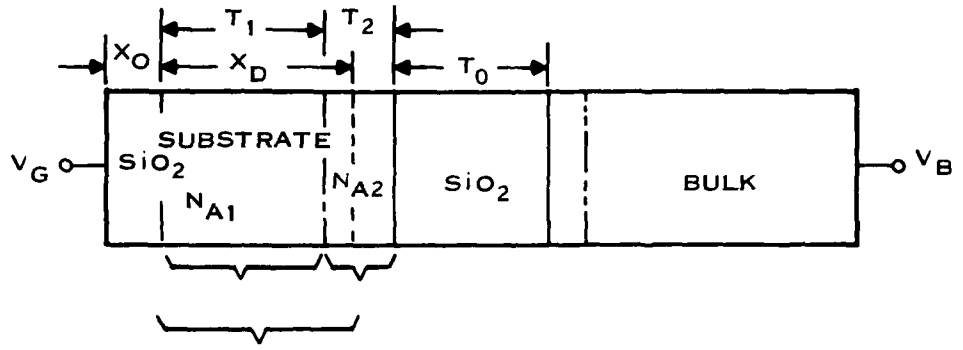
$$x_D = \left[V_G - \left(\phi_{GX} - \frac{Q_{f1}}{C_o}\right) - V_B + \left(\phi_{BX} - \frac{Q_{f2}}{C_{ob}}\right) + \phi_b + \frac{q}{2\epsilon_s}(N_{A2} - N_{A1})t_1^2 + \frac{q}{C_o}(N_{A2} - N_{A1})t_1 + qN_{A2}t_s\left(\frac{1}{2C_s} + \frac{1}{C_{ob}}\right)\right] \Big/ \left[qN_{A2}\left(\frac{1}{C_o} + \frac{1}{C_{ob}} + \frac{1}{C_s}\right)\right] \tag{D–3}$$

The device threshold voltage can be defined as

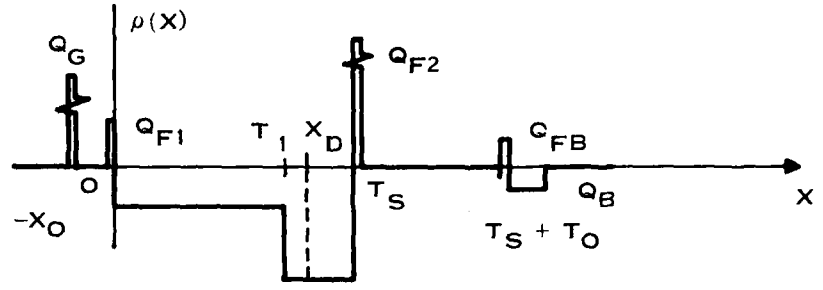
$$V_T = V_S + 2\phi_{F1} + \phi_{GX} - \frac{Q_{f1}}{C_o} + \frac{Q_D}{C_o} \tag{D–4}$$

where

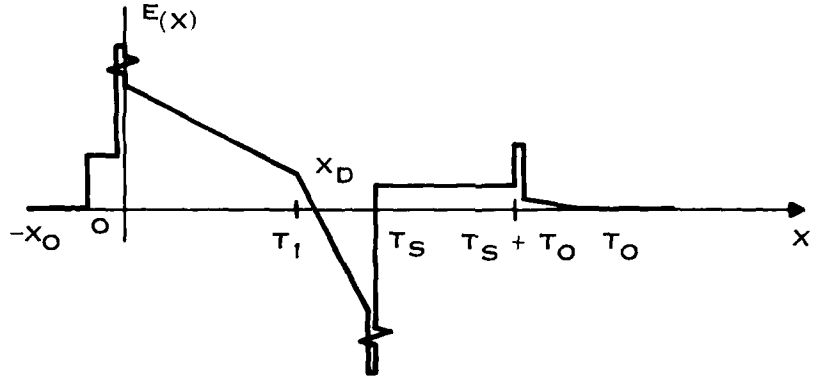
$$Q_D = -q(N_{A2} - N_{A1})t_1 + qN_{A2}x_D|_{V_G = V_T} \tag{D–5}$$



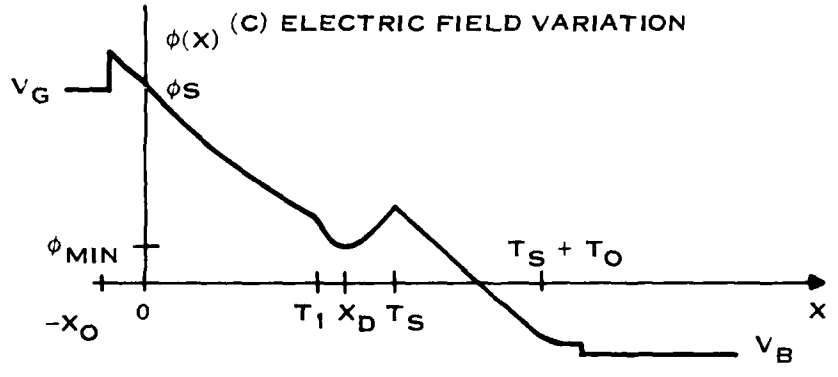
(A) ELEMENTAL SECTION OF DEVICE UNDER SPACE CHARGE INTERACTION



(B) CHARGE DENSITY



(C) ELECTRIC FIELD VARIATION



(D) POTENTIAL PROFILE

Figure D-1. Channel Depletion Interaction With Back Interface Depletion Region

Manipulation of Equations (D–3), (D–4), and (D–5) obtains

$$V_T = \left[V_G - \left(\phi_{GA} - \frac{Q_{f1}}{C_o} \right) - V_B + \left(\phi_{BA} - \frac{Q_{f2}}{C_{ob}} \right) + \phi_b + \frac{q}{2\epsilon_s} (N_{A2} - N_{A1})\, t_1^2 \right.$$

$$+ \frac{q}{C_o} (N_{A2} - N_{A1})\, t_1 + qN_{A2}\, t_s \left(\frac{1}{2C_s} + \frac{1}{C_{ob}} \right) - \left(\phi_{GA} - \frac{Q_{f1}}{C_o} \right) - V_B + \phi_b \qquad \text{(D–6)}$$

$$\left. + \left(\phi_{BA} - \frac{Q_{f2}}{C_{ob}} \right) \right] \Bigg/ \left(1 - \frac{C_c}{C_o} \right)$$

where

$$C_c = \left(\frac{1}{C_o} + \frac{1}{C_s} + \frac{1}{C_{ob}} \right)^{-1}$$

It is clear from Equation (D–6) that under space charge interaction, the threshold voltage assumes dependence on various parameters that are absent otherwise. Consequently, the threshold voltage control becomes more arduous.

APPENDIX E

ELECTROSTATICS OF A STEP DOPING PROFILE UNDER SPACE CHARGE INTERACTION

With the aid of Figure D–1, the use of Kirchoff's voltage law and Gauss's law gives

$$\phi_s = \phi_{min} + \frac{qN_{A2}}{2\epsilon_s}(x_D^2 - t_1^2) + \frac{qN_{A1}}{2\epsilon_s} t_1^2 \tag{E-1}$$

Elimination of ϕ_{min} from Equations (E–1) and (D–2) obtains

$$x_D = (\phi_s + \phi_B) \cdot \frac{C_m}{qN_{A2}} \tag{E-2}$$

where

$$C_m = \left(\frac{1}{C_{ob}} + \frac{1}{C_s}\right)^{-1}$$

$$\phi_B = \frac{q}{2\epsilon_s}(N_{A2} - N_{A1})\, t_1^2 + \frac{q}{2\epsilon_s} N_{A2}\, t_s^2 + \frac{q}{C_{ob}} N_{A2}\, t_s + \phi_{BX} - \frac{Q_{f2}}{C_{ob}} - \phi_b - V_B$$

The depletion charge that communicates with the gate can be written as

$$Q_D = qN_{A2}(x_D - t_1) + qN_{A1}\, t_1 \tag{E-3}$$

Using Equation (E–2) in Equation (E–3)

$$Q_D = \phi_s C_m + Q_{Di} \tag{E-4}$$

where $Q_{Di} = \phi_B C_m - q(N_{A2} - N_{A1})\, t_1$.

APPENDIX F

CALCULATION OF ϕ_{ss} AND ϕ_{sd}

The accurate calculation of the surface potentials on the source and drain ends of the channel is intrinsic to obtaining a model that remains continuously valid from weak inversion to strong inversion, from presaturation to postsaturation, without having to resort to their separate treatment. This can be accomplished by iterative solution of the exact charge neutrality equation at either end of the channel.[17,18]

The exact charge neutrality Equation (A-11)[17] can be simplified, Equation (B-8).[18] After modifications for a step doping profile, it can be expressed as

$$(V_g - \phi_s) = \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o}\left[\frac{kT}{q}\exp\left\{\frac{\phi_s - V_A - 2\phi_{F1}}{\frac{kT}{q}}\right\} + (\phi_s - \phi_t) + \frac{N_{A2}}{N_{A1}}(\phi_t - \phi_o)\right]^{1/2} \tag{F-1}$$

where V_A is the applied voltage at the terminal of interest, which is V_S and V_D at source and drain, respectively; ϕ_t is the potential at transition from region II to region I; and ϕ_o is the potential at the edge of the depletion layer that communicates with the gate terminal.

As ϕ_t and ϕ_o depend on the particular regime of operation, dicussed in Section III, Equation (F-1) will differ in each case.

I. CHANNEL DEPLETION LAYER CONFINED TO REGION I

In this regime of operation

$$\phi_t = \phi_o = V_X \tag{F-2}$$

therefore,

$$(V_g - \phi_s) = \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o}\left[\frac{kT}{q}\exp\frac{\phi_s - V_A - 2\phi_{F1}}{\frac{kT}{q}} + \phi_s - V_s\right]^{1/2} \tag{F-3}$$

II. CHANNEL DEPLETION LAYER EXTENDS IN REGION II

In this case

$$\phi_o = V_X \tag{F-4}$$

$$\phi_t = V_X + \frac{qN_{A2}}{2\epsilon_s}(x_D - t_1)^2 \tag{F-5}$$

Using Equation (B-4) in Equation (F-5)

$$\phi_t = \phi_s - \frac{qN_{A1}}{2\epsilon_s}t_1^2 + \frac{qN_{A2}}{\epsilon_s}t_1^2 - \frac{qN_{A2}}{\epsilon_s}t_1 \cdot \left\{\frac{2\epsilon_s}{qN_{A2}}\left(\phi_s - V_X - \frac{qN_{A2}t_1^2}{2\epsilon_s}\right) + t_1^2\right\}^{1/2} \tag{F-6}$$

Putting Equations (F–4) and (F–6) in Equation (F–1)

$$(V_g - \phi_s) = \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o}\left[\frac{kT}{q}\exp\frac{(\phi_s - V_A - 2\phi_{F1})}{\frac{kT}{q}} + \frac{N_{A2}}{N_{A1}}(\phi_s - V_X) - \left(\frac{N_{A2}}{N_{A1}} - 1\right)\right.$$
$$\left.\cdot\left\{\frac{qN_{A1}}{2\epsilon_s}t_1^2 - \frac{qN_{A2}}{\epsilon_s}t_1^2 + \frac{qN_{A2}}{\epsilon_s}t_1\cdot\left[\frac{2\epsilon_s}{qN_{A2}}\left(\phi_s - V_X - \frac{qN_{A1}}{2\epsilon_s}t_1^2\right) + t_1^2\right]^{1/2}\right\}\right]^{1/2} \quad \text{(F–7)}$$

III. CHANNEL DEPLETION LAYER INTERACTS WITH BACK INTERFACE DEPLETION CHARGE

In this mode of operation

$$\phi_o = \phi_{min} \quad \text{(F–8)}$$

$$\phi_t = \frac{qN_{A1}}{2\epsilon_s}(x_D - t_1)^2 + \phi_{min} \quad \text{(F–9)}$$

From Equations (E–1) and (E–2)

$$\phi_{min} = \phi_s - \frac{qN_{A1}}{2\epsilon_s}t_1^2 + \frac{qN_{A2}}{2\epsilon_s}t_1^2 - \frac{qN_{A2}}{2\epsilon_s}\left\{(\phi_s + \phi_B)\frac{C_m}{qN_{A2}}\right\}^2 \quad \text{(F–10)}$$

From Equations (E–2), (F–8) and (F–9)

$$\phi_t = \frac{qN_{A2}}{2\epsilon_s}\left[(\phi_s + \phi_B)\frac{C_m}{qN_{A2}} - t_1\right]^2 + \phi_s - \frac{qN_{A1}}{2\epsilon_s}t_1^2 + \frac{qN_{A2}}{2\epsilon_s}t_1^2 - \frac{qN_{A2}}{2\epsilon_s}\left\{(\phi_s + \phi_B)\frac{C_m}{qN_{A2}}\right\}^2 \quad \text{(F–11)}$$

Putting Equations (F–7) and (F–10) in Equation (F–1)

$$(V_g - \phi_s) = \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o}\left[\frac{kT}{q}\cdot\exp\left(\frac{\phi_s - V_A - 2\phi_{F1}}{\frac{kT}{q}}\right) + \frac{qN_{A1}}{2\epsilon_s}t_1^2\right.$$
$$\left. - \frac{qN_{A2}}{\epsilon_s}t_1^2 + (\phi_s + \phi_L)\frac{C_m t_1}{\epsilon_s} + \frac{qN_{A2}^2}{2\epsilon_s N_{A1}}\left\{(\phi_s + \phi_B)\frac{C_m}{qN_{A2}} - t_1\right\}^2\right]^{1/2} \quad \text{(F–12)}$$

IV. CHANNEL DEPLETION LAYER EXHAUSTS THE SUBSTRATE

From the solution of Poisson's equation and using Gauss's law and Kirchoff's voltage law, the following equations are pertinent to this condition.

$$\phi_s = \phi_o + E_o t_s + \frac{qN_{A2}}{2\epsilon_s}t_2^2 + \frac{qN_{A1}}{2\epsilon_s}t_1^2 + \frac{qN_{A2}}{2\epsilon_s}t_1 t_2 \quad \text{(F–13)}$$

$$V_B = \phi_o + \phi_{BX} + \phi_b - \frac{Q_{f2}}{C_{ob}} - \frac{\epsilon_s E_o}{C_{ob}} \qquad \text{(F-14)}$$

Simultaneous solution of Equations (F–13) and (F–14) provides

$$E_o = \frac{\phi_s - \phi_2}{t_s + \frac{\epsilon_s}{C_{ob}}} \qquad \text{(F-15)}$$

$$\phi_o = V_B - \phi_{BX} - \phi_b + \frac{Q_{f2}}{C_{ob}} + \frac{C_m}{C_{ob}}(\phi_s - \phi_2) \qquad \text{(F-16)}$$

Now

$$\begin{aligned} \phi_t &= \phi_o + E_o t_2 + \frac{qN_{A2} t_2^2}{2\epsilon_s} \\ &= V_B - \phi_{BX} - \phi_b + \frac{Q_{f2}}{C_{ob}} + \frac{C_m}{C_{ob}}(\phi_s - \phi_2) + \frac{(\phi_s - \phi_2) t_2}{t_s + \frac{\epsilon_s}{C_{ob}}} + \frac{qN_{A2} t_2^2}{2\epsilon_s} \end{aligned} \qquad \text{(F-17)}$$

Putting Equations (F–16) and (F–17) in Equation (F–1)

$$\begin{aligned} (V_g - \phi_s) = \frac{(2\epsilon_s qN_{A1})^{1/2}}{C_o}\Bigg[& \frac{kT}{q} \cdot \exp\left(\frac{\phi_s - V_A - 2\phi_{F1}}{\frac{kT}{q}}\right) \\ & + \phi_s - V_B + \phi_{BX} + \phi_b - \frac{Q_{f2}}{C_{ob}} - \frac{C_m}{C_{ob}}(\phi_s - \phi_2) - t_2 \cdot \frac{\phi_s - \phi_2}{t_s + \frac{\epsilon_s}{C_{ob}}} \\ & - \frac{qN_{A2} t_2^2}{2\epsilon_s} + \frac{N_{A2}}{N_{A1}}\left\{\frac{t_2(\phi_s - \phi_2)}{t_s + \frac{\epsilon_s}{C_{ob}}} + \frac{qN_{A2} t_2^2}{2\epsilon_s}\right\}\Bigg]^{1/2} \end{aligned} \qquad \text{(F-18)}$$

APPENDIX G

BURIED-CHANNEL COMPUTER PROGRAM FOR LONG-CHANNEL DEVICES

```
&BCMOS T=00004 IS ON CR00009 USING 00065 BLKS R=0000

0001    FTN4X
0002            SUBROUTINE BCMOS(ID,VDS,VGS,VBS,W,L,TOX,XI,NA,ND,TEMP,VFB,VDSAT,
0003           1REGION,SURF1,VT,VTIS,VTID,MU,FS)
0004            IMPLICIT REAL(A-Z)
0005            INTEGER NEASC(3),VBIASC(3),COXASC(3),NIASC(3),VKTASC(3),CIASC(3)
0006            INTEGER IDBSC(5),VDSBSC(5),VGSBSC(5),VBSBSC(5),REBSC(5),SUBSC(5)
0007            INTEGER VTBSC(5),VTSBSC(5),VTDBSC(5),MUBSC(5),VDBSC(5),FSBSC(5)
0008            INTEGER ASAT(5),ALIN(5),ASVT(5)
0009            DATA VDSBSC/2H   ,2H  V,2HDS,2H   ,2H    ,IDBSC/2H   ,2H   ,2HID,2H   ,
0010           12H   ,REBSC/2H   ,2HRE,2HGI,2HON,2H   /
0011            DATA VGSBSC/2H   ,2H  V,2HGS,2H   ,2H    /,VTBSC/2H(   ,2H   ,2HVT,2H   ,
0012           12H  ),SUBSC/2H   ,2H  S,2HUR,2HFX,2H   /
0013            DATA VBSBSC/2H   ,2H  V,2HBS,2H   ,2H    /,MUBSC/2H(   ,2H   ,2HID,2H   ,
0014           12H  ),VDBSC/2H(   ,2H  V,2HDBS,2HAT,2H  )/
0015            DATA VTSBSC/2H(   ,2H  V,2HTI,2HS   ,2H  )/,VTDBSC/2H(   ,2H  V,2HTI,2HD   ,
0016           12H  )/,FSBSC/2H(   ,2H   ,2HFS,2H   ,2H  )/
0017            DATA ASVT/2H   ,2HSU,2HB   ,2HVT,2H   /,ASAT/2HSA,2HTU,2HRA,2HTI,2HON/
0018            DATA ALIN/2H   ,2HLI,2HNE,2HAR,2H   /
0019            DATA NEASC/2HNE,2H   ,2H   /,VBIASC/2HVB,2HI   ,2H   /,COXASC/2HCO,
0020           12HX,  2H   /,NIASC/2HNI,2H   ,2H   /,VKTASC/2HVK,2HT   ,2H   /,CIASC/
0021           12HCI,2H   ,2H   /
0022    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0023    C                                                                       C
0024    C       THIS SUBROUTINE CALCULATES THE CURRENT FOR A BURIED CHANNEL     C
0025    C       MOSFET. IT CALLS THE FOLLOWING SUBROUTINES:                     C
0026    C                                                                       C
0027    C       SUBROUTINE SURFX(SURF,VDS,VGS,VFB,VTIS,VTID)                    C
0028    C       SUBROUTINE SATV(VDSAT,SURF,VGS,VBS,VBI,VFB,VT,VC,Q,ND,XI,KN,KE) C
0029    C       SUBROUTINE SURFQ(QVSD,QVSA,SURF,VDS,VGS,VBS,VBI,VFB,VC,KN,COX)  C
0030    C       SUBROUTINE MOBIL(MU,SURF)                                       C
0031    C                                                                       C
0032    C       THIS SECTION CALCULATES UNIT CONVERSIONS FOR INPUTS AND         C
0033    C       PARAMETERS WHICH WILL REMAIN CONSTANT. THESE CALCULATES ARE     C
0034    C       DONE ONLY ON THE FIRST PASS THROUGH THE PROGRAM.                C
0035    C                                                                       C
0036    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0037            IF(REGION.GT.0.0)GO TO 10
0038            EPSSI=1.04E-12
0039            EPSOX=3.455E-13
0040            Q=1.6E-19
0041            WEFF=W*1.0E-4
0042            LEFF=L*1.0E-4
0043            XI=XI*1.0E-4
0044            TOX=TOX*1.0E-8
0045            NE=NA*ND/(NA+ND)
0046            KN=SQRT(2.0*EPSSI*Q*ND)
0047            KE=SQRT(2.0*EPSSI*Q*NE)
0048            VKT=8.62E-5*TEMP
```

```
0049            NI=3.88E16*TEMP**1.5*EXP(-7000./TEMP)
0050            VBI=VKT*ALOG(NA*ND/NI/NI)
0051            COX=EPSOX/TOX
0052            CI=EPSSI/XI
0053            VC=Q*ND*EPSSI*2.0/COX/COX
0054            WRITE(6,23)
0055    23      FORMAT(/"COMPUTED VALUES"//)
0056            WRITE(6,2)NEASC,NE,VBIASC,VBI,COXASC,COX
0057            WRITE(6,2)NIASC,NI,VKTASC,VKT,CIASC,CI
0058    2       FORMAT(3(3A2,"=",E10,.4,5X,:))
0059            WRITE(6,19)
0060    19      FORMAT(/" ")
0061            WRITE(6,20) IDBSC,VDSBSC,VGSBSC,VBSBSC,REBSC,SUBSC
0062            WRITE(6,20) VTBSC,VTSBSC,VTDBSC,MUBSC,VDBSC,FSBSC
0063    20      FORMAT(1X,(6(5A2," | ",:)))
0064            WRITE(6,21)
0065    21      FORMAT(70"*"/)
0066    C
0067    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0068    C                                                                       C
0069    C       IN THIS SECTION CALCULATE THE THRESHOLD VOLTAGES. THEN          C
0070    C       DETERMINE IF THE DEVICE IS ABOVE THRESHOLD. IF NOT, BRANCH      C
0071    C       TO THE SUBTHRESHOLD REGION.                                     C
0072    C                                                                       C
0073    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0074    10      VT=VFB-(1.0/COX+0.5/CI)*Q*ND*XI+(1.0/COX+1.0/CI)*KE*SQRT(VBS+VBI)
0075           1-NE/ND*(VBS+VBI)
0076            VTIS=VFB-VBS-VBI-KN*(SQRT(VBS+VBI)/COX
0077            VTID=VFB-VBS-VBI-KN*SQRT(VDS+VBS+VBI)/COX
0078            IF(VGS.GT.VT)GO TO 100
0079            IF(VT.LT.VTIS)GO TO 100
0080            GO TO 1000
0081    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0082    C                                                                       C
0083    C       NOW SELF-CONSISTENTLY DETERMINE THE CONDITION OF THE SURFACE    C
0084    C       AND THE SATURATION VOLTAGE.                                     C
0085    C                                                                       C
0086    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0087    100     CALL SURFX(SURF1,VDS,VGS,VFB,VTIS,VTID)
0088    200     CALL SATV(VDSAT,SURF1,VGS,VBS,VBI,VFB,VT,VC,Q,ND,XI,KN,KE)
0089            VTID=VFB-VBS-VBI-KN*SQRT(VDSAT+VBS+VBI)/COX
0090            IF(VDS.LE.VDSAT)GO TO 2000
0091            CALL SURFX(SURF2,VDSAT,VGS,VFB,VTIS,VTID)
0092            IF(SURF1.EQ.SURF2)GO TO 3000
0093            SURF1=0.0
0094    220     CALL SATV(VDSAT,SURF1,VGS,VBS,VBI,VFB,VT,VC,Q,ND,XI,KN,KE)
0095            VTID=VFB-VBS-VBI-KN*SQRT(VDSAT+VBS+VBI)/COX
0096            CALL SURFX(SURF2,VDSAT,VGS,VFB,VTIS,VTID)
0097            IF(SURF1.EQ.SURF2)GO TO 3000
0098            SURF1=SURF1+1.0
0099            IF(SURF1.LT.6.0)GO TO 220
0100            WRITE(6,250)
0101    250     FORMAT(1X,"THIS IS STATEMENT 250 IN BCMOS")
0102            GO TO 4000
```

```
0103    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0104    C                                                                      C
0105    C       THIS IS THE SUBTHRESHOLD REGION OF OPERATION WHICH HAS NOT     C
0106    C       BEEN DEVELOPED YET.                                            C
0107    C                                                                      C
0108    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0109    1000    ID=0.0
0110            REGION=1.0
0111            SURF1=0.0
0112            FS=0.0
0113            GO TO 4000
0114    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0115    C                                                                      C
0116    C       EVALUATE LINEAR REGION CURRENT AND RETURN.                     C
0117    C                                                                      C
0118    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0119    2000    REGION=2.0
0120            CALL SURFQ(QVSD,QVSA,SURF1,VDS,VGS,VBS,VBI,VFB,VC,KN,COX)
0121            CALL MOBIL(MUB,MUS,SURF1)
0122            ID=WEFF*MUB/LEFF*(Q*ND*XI*VDS-2.0/3.0*KE*((VDS+VBS+VBI)**1.5
0123           1-(VBS+VBI)**1.5)-QVSD-MUS/MUB*QVSA)
0124            FS=QVSD+QVSA
0125            GO TO 4000
0126    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0127    C                                                                      C
0128    C       EVALUATE THE SATURATION REGION CURRENT AND RETURN.             C
0129    C                                                                      C
0130    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0131    3000    REGION=3.0
0132            CALL SURFQ(QVSD,QVSA,SURF1,VDSAT,VGS,VBS,VBI,VFB,VC,KN,COX)
0133            CALL MOBIL(MUB,MUS,SURF1)
0134            ID=WEFF*MUB/LEFF*(Q*ND*XI*VDSAT-2.0/3.0*KE*((VDSAT+VBS+VBI)**1.5
0135           1-(VBS+VBI)**1.5)-QVSD-MUS/MUB*QVSA)
0136            FS=QVSD+QVSA
0137    4000    VBS=VDS
0138            VDS=VGS+10.0
0139            VGS=VBS
0140            RETURN
0141            END
0142    C
0143    C ***********************************************************************************************
0144    C ***********************************************************************************************
0145    C ***********************************************************************************************
0146    C ***********************************************************************************************
0147    C
0148            SUBROUTINE SURFX(SURF,VDS,VGS,VFB,VTIS,VTID)
0149            IMPLICIT REAL(A-Z)
0150    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0151    C                                                                      C
0152    C       INVERSION ALONG ENTIRE SURFACE.                                C
0153    C                                                                      C
0154    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0155            IF(VGS.GT.VTID)GO TO 200
0156            SURF=1.0
0157            GO TO 999
```

```
0158  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0159  C                                                                      C
0160  C        INVERSION AT SOURCE - DEPLETION AT DRAIN                      C
0161  C                                                                      C
0162  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0163  200     IF(VGS.GT.VTIS)GO TO 300
0164          SURF=2.0
0165          GO TO 999
0166  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0167  C                                                                      C
0168  C        DEPLETION ALONG ENTIRE CHANNEL                                C
0169  C                                                                      C
0170  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0171  300     IF(VGS.GT.VFB)GO TO 400
0172          SURF=3.0
0173          GO TO 999
0174  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0175  C                                                                      C
0176  C        ACCUMULATION AT SOURCE - DEPLETION AT DRAIN                   C
0177  C                                                                      C
0178  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0179  400    VCOMP=VFB+VDS
0180          IF(VGS.GT.VCOMP)GO TO 500
0181          SURF=4.0
0182          GO TO 999
0183  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0184  C                                                                      C
0185  C        ACCUMULATION ALONG ENTIRE SURFACE                             C
0186  C                                                                      C
0187  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0188  500     SURF=5.0
0189  999     RETURN
0190          END
0191  C
0192  C
0193  C
0194          SUBROUTINE SATV(VDSAT,SURF,VGS,VBS,VBI,VFB,VT,VC,Q,ND,XI,KN,KE)
0195          IMPLICIT REAL(A-Z)
0196  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0197  C                                                                      C
0198  C        INVERSION AT DRAIN                                            C
0199  C                                                                      C
0200  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0201          IF(SURF.NE.1.0)GO TO 500
0202          VDSAT=(Q*ND*XI/(KN+KE))**2.0-VBS-VBI
0203          GO TO 999
0204  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0205  C                                                                      C
0206  C        ACCUMULATION AT DRAIN - SATURATION SUPPOSEDLY WILL NOT         C
0207  C        OCCUR IN A LONG CHANNEL DEVICE.                               C
0208  C                                                                      C
0209  CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0210  500     IF(SURF.NE.5.0)GO TO 200
0211          VDSAT=99.99
0212          GO TO 999
```

```
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                    C
C         DEPLETION AT DRAIN                                         C
C                                                                    C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
200     X1=0.0
        ARGX1=X1-VGS+VFB+VC
        IF(ARGX1.LT.0.0)ARGX1=0.0
        F1=(Q*ND*XI/KE-KN/KE*(SQRT(ARGX1)-SQRT(VC)))**2.0-VBS-VBI-X1
        X2=VGS-VT
        ARGX2=X2-VGS+VFB+VC
        IF(ARGX2.LT.0.0)ARGX2=0.0
        F2=(Q*ND*XI/KE-KN/KE*(SQRT(ARGX2)-SQRT(VC)))**2.0-VBS-VBI-X2
        LOOP3=0.0
380     DELTX=(X2-X1)/2.0
        LOOP3=LOOP3+1.0
        XX=X1+DELTX
        ARGX=XX-VGS+VFB+VC
        IF(ARGX.LT.0.0)ARGX=0.0
        FX=(Q*ND*XI/KE-KN/KE*(SQRT(ARGX)-SQRT(VC)))**2.0-VBS-VBI-XX
        RATIO=FX/F2
        IF(RATIO.GT.0.0)GO TO 390
        X1=XX
        F1=FX
        GO TO 400
390     X2=XX
        F2=FX
400     ERROR=DELTX/X1
        IF(ERROR.GT.0.02)GO TO 380
        VDSAT=(X1+X2)/2.0
999     RETURN
        END
C
C
C
        SUBROUTINE SURFQ(QVSD,QVSA,SURF,VDS,VGS,VBS,VBI,VFB,VC,KN,COX)
        IMPLICIT REAL(A-Z)
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                    C
C         INVERSION ALONG ENTIRE SURFACE                             C
C                                                                    C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
        IF(SURF.NE.1.0)GO TO 200
        QVSD=2.0/3.0*KN*((VDS+VBS+VBI)**1.5-(VBS+VBI)**1.5)
        QVSA=0.0
        GO TO 999
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                    C
C         INVERSION AT SOURCE - DEPLETION AT DRAIN                   C
C                                                                    C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
200     IF(SURF.NE.2.0)GO TO 300
        VID=(COX*(VGS+VBS-VFB+VBI)/KN)**2.0
        QVSD=2.0/3.0*KN*(VID**1.5-(VBS+VBI)**1.5+(VDS-VGS+VFB+VC)**1.5
       1-(VID-VGS-VBS+VFB-VBI+VC)**1.5-1.5*SQRT(VC)*(VDS+VBS+VBI-VID))
        QVSA=0.0
        GO TO 999
```

```
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                 C
C          DEPLETION ALONG ENTIRE SURFACE                         C
C                                                                 C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
300     IF(SURF.NE.3.0)GO TO 400
        QVSD=2.0/3.0*KN*((VDS-VGS+VFB+VC)**1.5-(-VGS+VFB+VC)**1.5
       1-1.5*SQRT(VC)*VDS)
        QVSA=0.0
        GO TO 999
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                 C
C          ACCUMULATION AT SOURCE - DEPLETION AT DRAIN            C
C                                                                 C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
400     IF(SURF.NE.4.0)GO TO 500
        QVSD=2.0/3.0*KN*((VDS-VGS+VFB+VC)**1.5-VC**1.5
       1-1.5*SQRT(VC)*(VDS-VGS+VFB))
        QVSA=-COX/2.0*(VGS+VBS-VFB+VBI)**2.0-COX*(0.5*(VBS+VBI)**2.0
       1-(VBS+VBI)*(VFG-VFB+VBS+VBI))
        GO TO 999
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                 C
C          ACCUMULATION ALONG ENTIRE SURFACE                      C
C                                                                 C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
500     QVSA=COX*(0.5*(VDS+BVS+VBI)**2.0-0.5*(VBS+VBI)**2.0
       1-(VGS+VBS-VFB+VBI)*VDS)
        QVSD=0.0
999     RETURN
        END
C
C
C
        SUBROUTINE MOBIL(MUB,MUS,SURF)
        IMPLICIT REAL(A-Z)
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                 C
C          INVERSION ALONG ENTIRE SURFACE                         C
C                                                                 C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
        IF(SURF.NE.1.0)GO TO 200
        MUB=1350.
        MUS=650.
        GO TO 999
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                 C
C          INVERSION AT SOURCE - DEPLETION AT DRAIN               C
C                                                                 C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
200     IF(SURF.NE.2.0)GO TO 300
        MUB=1350.
        MUS=650.
        GO TO 999
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                 C
C          DEPLETION ALONG ENTIRE SURFACE                         C
C                                                                 C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
```

```
0329    300     IF(SURF.NE.3.0)GO TO 400
0330            MUB=1350.
0331            MUS=650.
0332            GO TO 999
0333    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0334    C                                                                     C
0335    C       ACCUMULATION AT SOURCE - DEPLETION AT DRAIN                   C
0336    C                                                                     C
0337    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0338    400     IF(SURF.NE.4.0)GO TO 500
0339            MUB=1350.
0340            MUS=650.
0341            GO TO 999
0342    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0343    C                                                                     C
0344    C       ACCUMULATION ALONG ENTIRE SURFACE                             C
0345    C                                                                     C
0346    CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
0347    500     MUS=650.
0348            MUB=1350.
0349    999     RETURN
0350            END
0351            END$
```

APPENDIX H

PROGRAM MANUAL FOR CHARGE-SHARING MOSFET PREDICTOR MODEL

I. INTRODUCTION

The charge-sharing model will predict the dc current-voltage characteristics for an n-channel MOSFET. The notation for the terminal voltages is shown in Figure H–1.

The program allows the current or the derivative of the current with respect to any input variable (voltage or processing parameter) to be calculated with respect to any input variable (voltage or processing parameter). This flexibility allows the user to study such things as the sensitivity of current on channel length as a function of channel length [$d(I_d)/d(L)$ versus L], transconductance as a function of oxide thickness [$d(I_d)/d(V_{GG})$ versus T_{OX}], or current as a function of silicon substrate concentration [I_d versus N_{SUB}], etc. This program is written in Fortran and is presently running on an HP–1000 under RTE–IVB.

Details of the physics of the model are in the main body of this report.

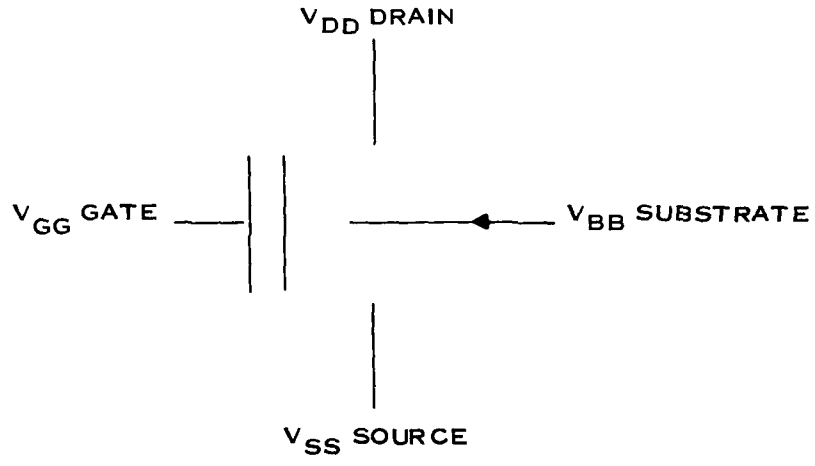


Figure H-1. Terminal Voltage Notation

II. USER'S GUIDE

1. Input Menu—QFORM

The file QFORM is a write-protected example input file. This file can be edited and stored in another NAMR. The form is designed to be read using EDIT in the screen mode but can be read and modified with a line editor. The first screen of QFORM is listed below and is the processing parameter input section. A description of the inputs follows the screen listing.

T1. PROCESSING PARAMETER INPUTS FOR CHARGE-SHARING MODEL

W → 5.0	NII → 5.E16	VFB0 → −0.9
WR → 1.2	XII → 0.10	TEMP → 300.
L → 2.5	NSUB → 5.E15	RHO → 20.
TOX → 300.0	XSUB → 0.43	RCONT → 50.
XJ → 0.4		
DELXJ → 0.65		
LS → 10.5		
LD → 10.5		

UNITS:

TOX → Angstroms	RHO → Ohms/Square
N1,N2,N3 → cm-3	RCONT → Ohms
NSUB → cm-3	DELXJ → Unitless
VFB0 → Volts	
TEMP → Kelvin	ALL OTHERS → Microns

Mnemonic	Description	Comments
		DEVICE GEOMETRY
W	mask width	
WR	width reduction	
L	mask lengtn	
TOX	gate oxide thickness	
XJ	source/drain junction depth	
DELXJ	fraction of XJ penetration under gate	
LS	distance from source contact to gate	
LD	distance from drain contact to gate	
		CHANNEL IMPLANT
NII	surface concentration of channel	
X1	distance to beginning of transition	
NSUB	substrate concentration	
XSUB	distance to end of transition	
		ELECTRICAL/MOBILITY
VFB0	flat band voltage	
TEMP	temperature – presently use only 300. ← ***	
RHO	source/drain sheet resistivity	

Mnemonic	Description	Comments
RCONT	source/drain contact resistance	
MU0	low field–low doping mobility	
THETA0	surface scattering for TOX = 500A	
ECMU	constant defining mobility curve	
EMAX	maximum electric field at drain	
XVDSF	fraction of VDS to calculate F	
VERROR	error tolerance for terminal voltages of intrinsic device	

The second screen of QFORM is used to define the terminal voltages and variables to be plotted. There are four terminals to the device, and the voltages, $V_{DD}, V_{GG}, V_{BB}, V_{SS}$, must be defined once and only once or an error message will be generated. It is also possible to select one of the processing parameters from the first screen as a variable to be plotted. If a processing variable is selected for plotting, the LOW-HIGH-STEP values will override the value entered in the first screen.

This program allows four variables to be stepped. The AXES ASSIGNMENT designates the intended use of the four stepped variables in the plotting program NPLOT. The XAXIS is the X-axis. FAMILY represents a set of curves, which are to be overlayed on the same plot. PRMTAR (parameter) and REFVAR (reference variable) are values that will be constant for a selected plot. Any combination of PRMTAR and REFVAR can be selected for plotting in the plot program NPLOT. FIXVAR (fixed variable) and FIXVAL (value of fixed variable) are only used when a processing parameter is designated as one of the AXES ASSIGNMENTs, leaving one terminal voltage unassigned. This unassigned voltage must be defined in the UNDEF TERMINAL (undefined terminal) section of screen two. The AXES ASSIGNMENTs are for some intended use and can be redesignated in the plotting program NPLOT for the data generated by this form.

Listed below is an example of the second screen of QFORM where L, the mask channel length, is plotted on the X-axis and the drain voltage is fixed at 0.5 V. Any processing parameter selected from screen one and designated as an AXES ASSIGNMENT will have the same units in screen two as it had in screen one. For this example L is stepped from 1.0 to 3.0 micrometers by +0.2-μm steps, V_{GG} is stepped from 1.0 to 3.0 V by +1.0-V steps, V_{BB} is stepped from 0.0 to −3.0 V by −1.0-V steps, and V_{SS} is held constant at 0.0 V. The sign of the STEP determines the role of LOW and HIGH as "start" and "stop."

T2. TERMINAL AND VOLTAGE ASSIGNMENTS FOR CHARGE-SHARING MODEL

Axes Assignment	Low	High	Step	UNDEF Terminal
XAXIS → L	1.0	3.0	0.2	FIXVAR → VDD
FAMILY → VGG	1.0	3.0	1.0	FIXVAL → 0.5
PRMTER → VBB	−3.0	0.0	−1.0	
REFVAR → VSS	0.0	0.0	0.0	

NOTES: The axes assignments can be the four terminals VDD, VGG, VBB, VSS or one of the terminals can be replaced by an input processing parameter from the previous menu. If one of the axes assignments is an input processing parameter, then one device terminal must be defined in the undefined terminal section by name = FIXVAR and by value = FIXVAL.

Another example for screen two is listed below. This example represents the standard I-V characteristics observed on a curve tracer for each substrate bias. V_{DD} is stepped from 0.0 to 5.0 V by 0.2-V steps, V_{GG} is stepped from 0.0 to 5.0 V by 1.0-V steps, V_{BB} is stepped from −3.0 to 0.0 V by +1.0-V steps (compare to previous example to see effect of step sign on start and stop values), and V_{SS} is held constant at 0.0 V.

T2. TERMINAL AND VOLTAGE ASSIGNMENTS FOR CHARGE-SHARING MODEL

Axes Assignment	Low	High	Step	UNDEF Terminal
XAXIS → VDD	0.0	5.0	0.2	FIXVAR →
FAMILY → VGG	0.0	5.0	1.0	FIXVAL →
PRMTAR → VBB	−3.0	0.0	1.0	
REFVAR → VSS	0.0	0.0	0.0	

NOTES: The axes assignments can be the four terminals VDD, VGG, VBB, VSS or one of the terminals can be replaced by an input processing parameter from the previous menu. If one of the axes assignments is an input processing parameter, then one device terminal must be defined in the undefined terminal section by name = FIXVAR and by value = IXVAL.

The third screen of QFORM controls the operation of the program. The FUNCTN (function) defines what the *Y*-axis of the plot will be. Presently, the current or the derivative of the current with respect to any variable, be it processing parameter or voltage, can be selected. VALUE1, VALUE2, and VALUE3 are defined by the function number selected. Additional functions that may use VALUE1, VALUE2, and VALUE3 can easily be added to the program. The CRT and PRINTR select where the printed output is to go. The CRT selection directs the output to the user's terminal and the user can map that terminal to an HP-9876A thermal printer to obtain a hard copy. The PRINTR selection directs the output to the line printer (LU = 6) at the HP-1000 site. Only those people at the computer site should insert "1" for PRINTR. OUTPUT FILE defines the file name, security code, and cartridge where the data is to be stored. The program will purge the file name and then create a new file with this name to store the data in. Thus, if the data is to be saved, the file must be renamed or the OUTPUT FILE must be changed.

Below is an example of the third screen where the current is selected for the *Y*-axis, the data is printed on both the terminal and the line printer, and the data to be plotted is to be stored in file DATAXX::31.

T3. CONTROL PARAMETERS FOR CHARGE-SHARING MODEL

FUNCTN → 1	← numeric field	CRT → 1 0 = no
VALUE1 →	← alpha field	PRINTR → 1 1 = yes
VALUE2 →	← alpha field	
VALUE3 →	← numeric field	OUTPUT FILE → DATAXX::31

Function #	Function Description
1	Plot Id on the Y-axis
2	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Percent Delta of VALUE2
3	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Actual Delta of VALUE2

Another example of the third screen is listed below where the numerical derivative of the current with respect to T_{OX} will be calculated for later plotting on the Y-axis. The numerical derivative will be calculated from

$$Y = \frac{I_d(T_{OX} + T_{OX}\text{*VALUE3/100.}) - I_d(T_{OX} - T_{OX}\text{*VALUE3/100})}{2.0\text{*}T_{OX}\text{*VALUE3/100.}}$$

It should be noted that T_{OX} may or may not be selected as an AXES ASSIGNMENT in the second screen. The value of T_{OX} present at the time of evaluation will be used to calculate the derivative whether it is being stepped or not. The data is not being output to either the terminal or the line printer but is being stored in file DATAYY::32 for later plotting.

T3. CONTROL PARAMETERS FOR CHARGE-SHARING MODEL

FUNCTN → 2	← numeric field	CRT → 0 0 = no
VALUE1 →	← alpha field	PRINTR → 0 1 = yes
VALUE2 → TOX	← alpha field	
VALUE3 → 1.0	← numeric field	OUTPUT FILE → DATAYY::32

Function #	Function Description
1	Plot Id on the Y-axis
2	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Percent Delta of VALUE2
3	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Actual Delta of VALUE2

2. Running the Program

To run the charge-sharing program, type "TR,RUQSHR" and then use the "RETURN" key. The program will then prompt you for the name of the input file you created from the QFORM example in Section II.1. Enter the file name; the name of the output file will be listed at the terminal when the program is finished.

3. Example 1, Line Printer Listing of "I_d Versus V_{DS}"

T1. PROCESSING PARAMETER INPUTS FOR CHARGE-SHARING MODEL

W → 5.0	NII → 3.E16	VFB0 → −0.9
WR → 1.2	XII → 0.05	TEMP → 300.
L → 2.5	NSUB → 1.E15	RHO → 20.
TOX → 300.0	XSUB → 0.43	RCONT → 50.
XJ → 0.4		
DELXJ → 0.65		
LS → 10.5		
LD → 10.5		

UNITS:

TOX → Angstroms	RHO → Ohms/Square
NII → cm-3	RCONT → Ohms
NSUB → cm-3	DELXJ → Unitless
VFB0 → Volts	
TEMP → Kelvin	ALL OTHERS → Microns

T2. TERMINAL AND VOLTAGE ASSIGNMENTS FOR CHARGE-SHARING MODEL

Axes Assignment	Low	High	Step	UNDEF Terminal
XAXIS → VDD	0.0	5.0	0.2	FIXVAR →
FAMILY → VGG	0.0	5.0	1.0	FIXVAL →
PRMTAR → VBB	−1.0	0.0	−1.0	
REFVAR → VSS	0.0	0.0	0.0	

NOTES: The axes assignment ... be the four terminals VDD, VGG, VBB, VSS or one of the terminals can be replaced by an input processing parameter from the previous menu. If one of the axes assignments is an input processing parameter, then one device terminal must be defined in the undefined terminal section by name = FIXVAR and by value = FIXVAL.

T3. CONTROL PARAMETERS FOR CHARGE-SHARING MODEL

FUNCTN → 1	← numeric field	CRT → 0 0 = no
VALUE1 →	← alpha field	PRINTR → 1 1 = yes
VALUE2 →	← alpha field	
VALUE3 →	← numeric field	OUTPUT FILE → DATAXX::31

Function #	Function Description
1	Plot Id on the Y-axis
2	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Percent Delta of VALUE2
3	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Actual Delta of VALUE2

COMPUTED VALUES

WEFF = 3.800	COX = 0.12E-06	VKT = 0.02586
LEFF = 1.480	RS = 92.00	NI = 0.15E+11
RJ = 0.260	RD = 81.30	TWOPF = 0.77254

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.0000E+00	0.000	0.000	0.000	SUB−VT	0.893
	(0.506)	(0.000)	(660.00)	(0.233E+17)	(0.205)
0.1863E−12	0.200	0.000	0.000	SUB−VT	0.889
	(0.506)	(0.000)	(598.56)	(0.233E+17)	(0.205)
0.1991E−12	0.400	0.000	0.000	SUB−VT	0.885
	(0.506)	(0.000)	(572.83)	(0.233E+17)	(0.205)
0.2120E−12	0.600	0.000	0.000	SUB−VT	0.881
	(0.506)	(0.000)	(549.65)	(0.233E+17)	(0.205)
0.2253E−12	0.800	0.000	0.000	SUB−VT	0.877
	(0.506)	(0.000)	(528.67)	(0.233E+17)	(0.205)
0.2390E−12	1.000	0.000	0.000	SUB−VT	0.873
	(0.506)	(0.000)	(509.58)	(0.233E+17)	(0.205)
0.2532E−12	1.200	0.000	0.000	SUB−VT	0.870
	(0.506)	(0.000)	(492.13)	(0.233E+17)	(0.205)
0.2678E−12	1.400	0.000	0.000	SUB−VT	0.866
	(0.506)	(0.000)	(476.12)	(0.233E+17)	(0.205)
0.2830E−12	1.600	0.000	0.000	SUB−VT	0.862
	(0.506)	(0.000)	(461.37)	(0.233E+17)	(0.205)
0.2987E−12	1.800	0.000	0.000	SUB−VT	0.859
	(0.506)	(0.000)	(447.75)	(0.233E+17)	(0.205)
0.3150E−12	2.000	0.000	0.000	SUB−VT	0.855
	(0.506)	(0.000)	(435.12)	(0.233E+17)	(0.205)
0.3320E−12	2.200	0.000	0.000	SUB−VT	0.852
	(0.506)	(0.000)	(423.38)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.3496E−12	2.400	0.000	0.000	SUB−VT	0.848
	(0.506)	(0.000)	(412.45)	(0.233E+17)	(0.205)
0.3679E−12	2.600	0.000	0.000	SUB−VT	0.845
	(0.506)	(0.000)	(402.24)	(0.233E+17)	(0.205)
0.3869E−12	2.800	0.000	0.000	SUB−VT	0.842
	(0.506)	(0.000)	(392.68)	(0.233E+17)	(0.205)
0.4067E−12	3.000	0.000	0.000	SUB−VT	0.838
	(0.506)	(0.000)	(383.72)	(0.233E+17)	(0.205)
0.4273E−12	3.200	0.000	0.000	SUB−VT	0.835
	(0.506)	(0.000)	(375.29)	(0.233E+17)	(0.205)
0.4488E−12	3.400	0.000	0.000	SUB−VT	0.832
	(0.506)	(0.000)	(367.37)	(0.233E+17)	(0.205)
0.4712E−12	3.600	0.000	0.000	SUB−VT	0.828
	(0.506)	(0.000)	(359.90)	(0.233E+17)	(0.205)
0.4946E−12	3.800	0.000	0.000	SUB−VT	0.825
	(0.506)	(0.000)	(352.85)	(0.233E+17)	(0.205)
0.5189E−12	4.000	0.000	0.000	SUB−VT	0.822
	(0.506)	(0.000)	(346.18)	(0.233E+17)	(0.205)
0.5443E−12	4.200	0.000	0.000	SUBVT	0.819
	(0.506)	(0.000)	(339.87)	(0.233E+17)	(0.205)
0.5707E−12	4.400	0.000	0.000	SUB−VT	0.816
	(0.506)	(0.000)	(333.88)	(0.233E+17)	(0.205)
0.5983E−12	4.600	0.000	0.000	SUB−VT	0.813
	(0.506)	(0.000)	(328.21)	(0.233E+17)	(0.205)
0.6272E−12	4.800	0.000	0.000	SUB−VT	0.810
	(0.506)	(0.000)	(322.82)	(0.233E+17)	(0.205)
0.6572E−12	5.000	0.000	0.000	SUB−VT	0.807
	(0.506)	(0.000)	(317.69)	(0.233E+17)	(0.205)
0.0000E+00	0.000	1.000	0.000	LINEAR	0.893
	(0.506)	(0.340)	(584.61)	(0.233E+17)	(0.205)
0.8961E−05	0.200	1.000	0.000	LINEAR	0.889
	(0.506)	(0.344)	(559.80)	(0.233E+17)	(0.205)
0.1111E−04	0.400	1.000	0.000	SATURATION	0.883
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1143E−04	0.600	1.000	0.000	SATURATION	0.873
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.1166E−04	0.800	1.000	0.000	SATURATION	0.865
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1185E−04	1.000	1.000	0.000	SATURATION	0.857
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1203E−04	1.200	1.000	0.000	SATURATION	0.850
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1219E−04	1.400	1 000	0.000	SATURATION	0.842
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1234E−04	1.600	1.000	0.000	SATURATION	0.835
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1248E−04	1.800	1.000	0.000	SATURATION	0.828
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1262E−04	2.000	1.000	0.000	SATURATION	0.820
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1275E−04	2.200	1.000	0.000	SATURATION	0.813
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1288E−04	2.400	1.000	0.000	SATURATION	0.806
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1301E−04	2.600	1.000	0.000	SATURATION	0.799
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1313E−04	2.800	1.000	0.000	SATURATION	0.792
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1325E−04	3.000	1.000	0.000	SATURATION	0.785
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1337E−04	3.200	1.000	0.000	SATURATION	0.778
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1348E−04	3.400	1.000	0.000	SATURATION	0.770
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1360E−04	3.600	1.000	0.000	SATURATION	0.763
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1371E−04	3.800	1.000	0.000	SATURATION	0.756
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1382E−04	4.000	1.000	0.000	SATURATION	0.749
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1393E−04	4.200	1.000	0.000	SATURATION	0.742
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.1404E−04	4.400	1.000	0.000	SATURATION	0.735
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1415E−04	4.600	1.000	0.000	SATURATION	0.728
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1426E−04	4.800	1.000	0.000	SATURATION	0.720
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.1437E−04	5.000	1.000	0.000	SATURATION	0.713
	(0.506)	(0.344)	(543.43)	(0.233E+17)	(0.205)
0.0000E+00	0.000	2.000	0.000	LINEAR	0.893
	(0.506)	(0.984)	(547.35)	(0.233E+17)	(0.205)
0.3165E−04	0.200	2.000	0.000	LINEAR	0.889
	(0.506)	(0.993)	(525.55)	(0.233E+17)	(0.205)
0.5495E−04	0.400	2.000	0.000	LINEAR	0.885
	(0.506)	(0.993)	(505.79)	(0.233E+17)	(0.205)
0.7107E−04	0.600	2.000	0.000	LINEAR	0.881
	(0.506)	(0.993)	(487.80)	(0.233E+17)	(0.205)
0.8091E−04	0.800	2.000	0.000	LINEAR	0.877
	(0.506)	(0.993)	(471.34)	(0.233E+17)	(0.205)
0.8526E−04	1.000	2.000	0.000	SATURATION	0.873
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.8743E−04	1.200	2.000	0.000	SATURATION	0.863
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.8898E−04	1.400	2.000	0.000	SATURATION	0.855
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9031E−04	1.600	2.000	0.000	SATURATION	0.848
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9152E−04	1.800	2.000	0.000	SATURATION	0.840
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9265E−04	2.000	2.000	0.000	SATURATION	0.833
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9371E−04	2.200	2.000	0.000	SATURATION	0.826
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9472E−04	2.400	2.000	0.000	SATURATION	0.819
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9570E−04	2.600	2.000	0.000	SATURATION	0.812
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.9665E−04	2.800	2.000	0.000	SATURATION	0.805
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9757E−04	3.000	2.000	0.000	SATURATION	0.798
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9846E−04	3.200	2.000	0.000	SATURATION	0.791
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.9934E−04	3.400	2.000	0.000	SATURATION	0.784
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.1002E−03	3.600	2.000	0.000	SATURATION	0.777
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.1011E−03	3.800	2.000	0.000	SATURATION	0.770
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.1019E−03	4.000	2.000	0.000	SATURATION	0.763
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.1027E−03	4.200	2.000	0.000	SATURATION	0.756
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.1035E−03	4.400	2.000	0.000	SATURATION	0.749
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.1043E−03	4.600	2.000	0.000	SATURATION	0.743
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.1051E−03	4.800	2.000	0.000	SATURATION	0.736
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.1059E−03	5.000	2.000	0.000	SATURATION	0.729
	(0.506)	(0.993)	(456.76)	(0.233E+17)	(0.205)
0.0000E+00	0.000	3.000	0.000	LINEAR	0.893
	(0.506)	(1.570)	(514.56)	(0.233E+17)	(0.205)
0.5172E−04	0.200	3.000	0.000	LINEAR	0.889
	(0.506)	(1.578)	(495.24)	(0.233E+17)	(0.205)
0.9413E−04	0.400	3.000	0.000	LINEAR	0.885
	(0.506)	(1.578)	(477.66)	(0.233E+17)	(0.205)
0.1285E−03	0.600	3.000	0.000	LINEAR	0.881
	(0.506)	(1.578)	(461.58)	(0.233E+17)	(0.205)
0.1557E−03	0.800	3.000	0.000	LINEAR	0.877
	(0.506)	(1.578)	(446.82)	(0.233E+17)	(0.205)
0.1766E−03	1.000	3.000	0.000	LINEAR	0.873
	(0.506)	(1.578)	(433.22)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.1919E−03	1.200	3.000	0.000	LINEAR	0.870
	(0.506)	(1.578)	(420.65)	(0.233E+17)	(0.205)
0.2021E−03	1.400	3.000	0.000	LINEAR	0.866
	(0.506)	(1.578)	(408.99)	(0.233E+17)	(0.205)
0.2079E−03	1.600	3.000	0.000	SATURATION	0.861
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2114E−03	1.800	3.000	0.000	SATURATION	0.853
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2140E−03	2.000	3.000	0.000	SATURATION	0.846
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2164E−03	2.200	3.000	0.000	SATURATION	0.840
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2186E−03	2.400	3.000	0.000	SATURATION	0.833
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2207E−03	2.600	3.000	0.000	SATURATION	0.826
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2226E−03	2.800	3.000	0.000	SATURATION	0.820
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2246E−03	3.000	3.000	0.000	SATURATION	0.813
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2264E−03	3.200	3.000	0.000	SATURATION	0.807
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2282E−03	3.400	3.000	0.000	SATURATION	0.801
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2300E−03	3.600	3.000	0.000	SATURATION	0.794
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2318E−03	3.800	3.000	0.000	SATURATION	0.788
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2335E−03	4.000	3.000	0.000	SATURATION	0.781
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2352E−03	4.200	3.000	0.000	SATURATION	0.775
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2368E−03	4.400	3.000	0.000	SATURATION	0.769
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2385E−03	4.600	3.000	0.000	SATURATION	0.762
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.2401E−03	4.800	3.000	0.000	SATURATION	0.756
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.2418E−03	5.000	3.000	0.000	SATURATION	0.749
	(0.506)	(1.578)	(399.28)	(0.233E+17)	(0.205)
0.0000E+00	0.000	4.000	0.000	LINEAR	0.893
	(0.506)	(2.107)	(485.48)	(0.233E+17)	(0.205)
0.6961E−04	0.200	4.000	0.000	LINEAR	0.889
	(0.506)	(2.115)	(468.24)	(0.233E+17)	(0.205)
0.1292E−03	0.400	4.000	0.000	LINEAR	0.885
	(0.506)	(2.115)	(452.49)	(0.233E+17)	(0.205)
0.1800E−03	0.600	4.000	0.000	LINEAR	0.881
	(0.506)	(2.115)	(438.04)	(0.233E+17)	(0.205)
0.2231E−03	0.800	4.000	0.000	LINEAR	0.877
	(0.506)	(2.115)	(424.73)	(0.233E+17)	(0.205)
0.2593E−03	1.000	4.000	0.000	LINEAR	0.873
	(0.506)	(2.115)	(412.42)	(0.233E+17)	(0.205)
0.2893E−03	1.200	4.000	0.000	LINEAR	0.870
	(0.506)	(2.115)	(401.01)	(0.233E+17)	(0.205)
0.3137E−03	1.400	4.000	0.000	LINEAR	0.866
	(0.506)	(2.115)	(390.40)	(0.233E+17)	(0.205)
0.3330E−03	1.600	4.000	0.000	LINEAR	0.862
	(0.506)	(2.115)	(380.51)	(0.233E+17)	(0.205)
0.3477E−03	1.800	4.000	0.000	LINEAR	0.859
	(0.506)	(2.115)	(371.26)	(0.233E+17)	(0.205)
0.3580E−03	2.000	4.000	0.000	LINEAR	0.855
	(0.506)	(2.115)	(362.60)	(0.233E+17)	(0.205)
0.3646E−03	2.200	4.000	0.000	SATURATION	0.850
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3684E−03	2.400	4.000	0.000	SATURATION	0.843
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3716E−03	2.600	4.000	0.000	SATURATION	0.837
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3746E−03	2.800	4.000	0.000	SATURATION	0.831
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3773E−03	3.000	4.000	0.000	SATURATION	0.825
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.3800E−03	3.200	4.000	0.000	SATURATION	0.819
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3825E−03	3.400	4.000	0.000	SATURATION	0.813
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3850E−03	3.600	4.000	0.000	SATURATION	0.808
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3874E−03	3.800	4.000	0.000	SATURATION	0.802
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3898E−03	4.000	4.000	0.000	SATURATION	0.796
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3922E−03	4.200	4.000	0.000	SATURATION	0.790
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3945E−03	4.400	4.000	0.000	SATURATION	0.785
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3967E−03	4.600	4.000	0.000	SATURATION	0.779
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.3990E−03	4.800	4.000	0.000	SATURATION	0.773
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.4012E−03	5.000	4.000	0.000	SATURATION	0.767
	(0.506)	(2.115)	(357.88)	(0.233E+17)	(0.205)
0.0000E+00	0.000	5.000	0.000	LINEAR	0.893
	(0.506)	(2.656)	(459.50)	(0.233E+17)	(0.205)
0.8564E−04	0.200	5.000	0.000	LINEAR	0.889
	(0.506)	(2.663)	(444.04)	(0.233E+17)	(0.205)
0.1607E−03	0.400	5.000	0.000	LINEAR	0.885
	(0.506)	(2.663)	(429.85)	(0.233E+17)	(0.205)
0.2266E−03	0.600	5.000	0.000	LINEAR	0.881
	(0.506)	(2.663)	(416.78)	(0.233E+17)	(0.205)
0.2842E−03	0.800	5.000	0.000	LINEAR	0.877
	(0.506)	(2.663)	(404.71)	(0.233E+17)	(0.205)
0.3344E−03	1.000	5.000	0.000	LINEAR	0.873
	(0.506)	(2.663)	(393.52)	(0.233E+17)	(0.205)
0.3780E−03	1.200	5.000	0.000	LINEAR	0.870
	(0.506)	(2.663)	(383.12)	(0.233E+17)	(0.205)
0.4156E−03	1.400	5.000	0.000	LINEAR	0.866
	(0.506)	(2.663)	(373.43)	(0.233E+17)	(0.205)

FUNCTN # 1	XAK (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.4477E−03	1.600	5.000	0.000	LINEAR	0.862
	(0.506)	(2.663)	(364.37)	(0.233E+17)	(0.205)
0.4748E−03	1.800	5.000	0.000	LINEAR	0.859
	(0.506)	(2.663)	(355.88)	(0.233E+17)	(0.205)
0.4973E−03	2.000	5.000	0.000	LINEAR	0.855
	(0.506)	(2.663)	(347.92)	(0.233E+17)	(0.205)
0.5155E−03	2.200	5.000	0.000	LINEAR	0.852
	(0.506)	(2.663)	(340.43)	(0.233E+17)	(0.205)
0.5298E−03	2.400	5.000	0.000	LINEAR	0.848
	(0.506)	(2.663)	(333.38)	(0.233E+17)	(0.205)
0.5403E−03	2.600	5.000	0.000	LINEAR	0.845
	(0.506)	(2.663)	(326.72)	(0.233E+17)	(0.205)
0.5469E−03	2.800	5.000	0.000	SATURATION	0.839
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5510E−03	3.000	5.000	0.000	SATURATION	0.833
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5545E−03	3.200	5.000	0.000	SATURATION	0.828
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5578E−03	3.400	5.000	0.000	SATURATION	0.822
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5609E−03	3.600	5.000	0.000	SATURATION	0.817
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5639E−03	3.800	5.000	0.000	SATURATION	0.812
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5668E−03	4.000	5.000	0.000	SATURATION	0.807
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5696E−03	4.200	5.000	0.000	SATURATION	0.801
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5723E−03	4.400	5.000	0.000	SATURATION	0.796
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5751E−03	4.600	5.000	0.000	SATURATION	0.791
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5777E−03	4.800	5.000	0.000	SATURATION	0.786
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)
0.5804E−03	5.000	5.000	0.000	SATURATION	0.781
	(0.506)	(2.663)	(324.70)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.0000E+00	0.000	0.000	−1.000	SUB−VT	0.816
	(0.773)	(2.663)	(627.30)	(0.886E+16)	(0.507)
0.1086E−17	0.200	0.000	−1.000	SUB−VT	0.812
	(0.773)	(2.663)	(622.37)	(0.886E+16)	(0.507)
0.1180E−17	0.400	0.000	−1.000	SUB−VT	0.809
	(0.773)	(2.663)	(599.22)	(0.886E+16)	(0.507)
0.1283E−17	0.600	0.000	−1.000	SUB−VT	0.805
	(0.773)	(2.663)	(578.13)	(0.886E+16)	(0.507)
0.1396E−17	0.800	0.000	−1.000	SUB−VT	0.802
	(0.773)	(2.663)	(558.85)	(0.886E+16)	(0.507)
0.1521E−17	1.000	0.000	−1.000	SUB−VT	0.798
	(0.773)	(2.663)	(541.19)	(0.886E+16)	(0.507)
0.1657E−17	1.200	0.000	−1.000	SUB−VT	0.794
	(0.773)	(2.663)	(524.97)	(0.886E+16)	(0.507)
0.1808E−17	1.400	0.000	−1.000	SUB−VT	0.790
	(0.773)	(2.663)	(510.04)	(0.886E+16)	(0.507)
0.1974E−17	1.600	0.000	−1.000	SUB−VT	0.786
	(0.773)	(2.663)	(496.28)	(0.886E+16)	(0.507)
0.2157E−17	1.800	0.000	−1.000	SUB−VT	0.781
	(0.773)	(2.663)	(483.57)	(0.886E+16)	(0.507)
0.2359E−17	2.000	0.000	−1.000	SUB−VT	0.777
	(0.773)	(2.663)	(471.80)	(0.886E+16)	(0.507)
0.2582E−17	2.200	0.000	−1.000	SUB−VT	0.773
	(0.773)	(2.663)	(460.90)	(0.886E+16)	(0.507)
0.2829E−17	2.400	0.000	−1.000	SUB−VT	0.768
	(0.773)	(2.663)	(450.78)	(0.886E+16)	(0.507)
0.3102E−17	2.600	0.000	−1.000	SUB−VT	0.764
	(0.773)	(2.663)	(441.37)	(0.886E+16)	(0.507)
0.3404E−17	2.800	0.000	−1.000	SUB−VT	0.759
	(0.773)	(2.663)	(432.63)	(0.886E+16)	(0.507)
0.3739E−17	3.000	0.000	−1.000	SUB−VT	0.755
	(0.773)	(2.663)	(424.48)	(0.886E+16)	(0.507)
0.4110E−17	3.200	0.000	−1.000	SUB−VT	0.750
	(0.773)	(2.663)	(416.89)	(0.886E+16)	(0.507)
0.4521E−17	3.400	0.000	−1.000	SUB−VT	0.745
	(0.773)	(2.663)	(409.82)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.4977E−17	3.600	0.000	−1.000	SUB−VT	0.740
	(0.773)	(2.663)	(403.22)	(0.886E+16)	(0.507)
0.5483E−17	3.800	0.000	−1.000	SUB−VT	0.736
	(0.773)	(2.663)	(397.06)	(0.886E+16)	(0.507)
0.6046E−17	4.000	0.000	−1.000	SUB−VT	0.731
	(0.773)	(2.663)	(391.31)	(0.886E+16)	(0.507)
0.6672E−17	4.200	0.000	−1.000	SUB−VT	0.726
	(0.773)	(2.663)	(385.94)	(0.886E+16)	(0.507)
0.7367E−17	4.400	0.000	−1.000	SUB−VT	0.721
	(0.773)	(2.663)	(380.93)	(0.886E+16)	(0.507)
0.8142E−17	4.600	0.000	−1.000	SUB−VT	0.716
	(0.773)	(2.663)	(376.26)	(0.886E+16)	(0.507)
0.9004E−17	4.800	0.000	−1.000	SUB−VT	0.711
	(0.773)	(2.663)	(371.90)	(0.886E+16)	(0.507)
0.9964E−17	5.000	0.000	−1.000	SUB−VT	0.706
	(0.773)	(2.663)	(367.83)	(0.886E+16)	(0.507)
0.0000E+00	0.000	1.000	−1.000	LINEAR	0.816
	(0.773)	(0.227)	(602.39)	(0.886E+16)	(0.507)
0.3029E−05	0.200	1.000	−1.000	SATURATION	0.812
	(0.773)	(0.196)	(580.94)	(0.886E+16)	(0.507)
0.3169E−05	0.400	1.000	−1.000	SATURATION	0.793
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3276E−05	0.600	1.000	−1.000	SATURATION	0.778
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3369E−05	0.800	1.000	−1.000	SATURATION	0.764
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3454E−05	1.000	1.000	−1.000	SATURATION	0.750
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3535E−05	1.200	1.000	−1.000	SATURATION	0.737
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3612E−05	1.400	1.000	−1.000	SATURATION	0.724
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3687E−05	1.600	1.000	−1.000	SATURATION	0.711
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3761E−05	1.800	1.000	−1.000	SATURATION	0.697
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.3834E−05	2.000	1.000	−1.000	SATURATION	0.684
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3905E−05	2.200	1.000	−1.000	SATURATION	0.670
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.3977E−05	2.400	1.000	−1.000	SATURATION	0.656
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4048E−05	2.600	1.000	−1.000	SATURATION	0.642
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4119E−05	2.800	1.000	−1.000	SATURATION	0.628
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4190E−05	3.000	1.000	−1.000	SATURATION	0.613
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4262E−05	3.200	1.000	−1.000	SATURATION	0.598
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4334E−05	3.400	1.000	−1.000	SATURATION	0.583
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4407E−05	3.600	1.000	−1.000	SATURATION	0.568
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4480E−05	3.800	1.000	−1.000	SATURATION	0.552
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4554E−05	4.000	1.000	−1.000	SATURATION	0.536
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4629E−05	4.200	1.000	−1.000	SATURATION	0.519
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4705E−05	4.400	1.000	−1.000	SATURATION	0.503
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4782E−05	4.600	1.000	−1.000	SATURATION	0.486
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4860E−05	4.800	1.000	−1.000	SATURATION	0.468
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.4940E−05	5.000	1.000	−1.000	SATURATION	0.451
	(0.773)	(0.196)	(580.97)	(0.886E+16)	(0.507)
0.0000E+00	0.000	2.000	−1.000	LINEAR	0.816
	(0.773)	(0.962)	(562.91)	(0.886E+16)	(0.507)
0.2688E−04	0.200	2.000	−1.000	LINEAR	0.812
	(0.773)	(0.970)	(543.75)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.4675E−04	0.400	2.000	−1.000	LINEAR	0.809
	(0.773)	(0.970)	(526.17)	(0.886E+16)	(0.507)
0.6044E−04	0.600	2.000	−1.000	LINEAR	0.805
	(0.773)	(0.970)	(510.00)	(0.886E+16)	(0.507)
0.6856E−04	0.800	2.000	−1.000	LINEAR	0.802
	(0.773)	(0.970)	(495.10)	(0.886E+16)	(0.507)
0.7191E−04	1.000	2.000	−1.000	SATURATION	0.795
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.7385E−04	1.200	2.000	−1.000	SATURATION	0.780
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.7542E−04	1.400	2.000	−1.000	SATURATION	0.768
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.7684E−04	1.600	2.000	−1.000	SATURATION	0.755
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.7818E−04	1.800	2.000	−1.000	SATURATION	0.744
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.7946E−04	2.000	2.000	−1.000	SATURATION	0.732
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.8071E−04	2.200	2.000	−1.000	SATURATION	0.720
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.8193E−04	2.400	2.000	−1.000	SATURATION	0.708
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.8313E−04	2.600	2.000	−1.000	SATURATION	0.695
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.8431E−04	2.800	2.000	−1.000	SATURATION	0.683
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.8549E−04	3.000	2.000	−1.000	SATURATION	0.671
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.8665E−04	3.200	2.000	−1.000	SATURATION	0.658
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.8781E−04	3.400	2.000	−1.000	SATURATION	0.645
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.8897E−04	3.600	2.000	−1.000	SATURATION	0.632
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.9013E−04	3.800	2.000	−1.000	SATURATION	0.619
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.9129E−04	4.000	2.000	−1.000	SATURATION	0.605
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.9244E−04	4.200	2.000	−1.000	SATURATION	0.591
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.9361E−04	4.400	2.000	−1.000	SATURATION	0.577
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.9477E−04	4.600	2.000	−1.000	SATURATION	0.563
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.9594E−04	4.800	2.000	−1.000	SATURATION	0.548
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.9712E−04	5.000	2.000	−1.000	SATURATION	0.534
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.0000E+00	0.000	3.000	−1.000	LINEAR	0.816
	(0.773)	(1.634)	(528.29)	(0.886E+16)	(0.507)
0.4789E−04	0.200	3.000	−1.000	LINEAR	0.812
	(0.773)	(1.642)	(511.38)	(0.886E+16)	(0.507)
0.8789E−04	0.400	3.000	−1.000	LINEAR	0.809
	(0.773)	(1.642)	(495.79)	(0.886E+16)	(0.507)
0.1209E−03	0.600	3.000	−1.000	LINEAR	0.805
	(0.773)	(1.642)	(481.41)	(0.886E+16)	(0.507)
0.1476E−03	0.800	3.000	−1.000	LINEAR	0.802
	(0.773)	(1.642)	(468.11)	(0.886E+16)	(0.507)
0.1686E−03	1.000	3.000	−1.000	LINEAR	0.798
	(0.773)	(1.642)	(455.80)	(0.886E+16)	(0.507)
0.1844E−03	1.200	3.000	−1.000	LINEAR	0.794
	(0.773)	(1.642)	(444.38)	(0.886E+16)	(0.507)
0.1954E−03	1.400	3.000	−1.000	LINEAR	0.790
	(0.773)	(1.642)	(433.77)	(0.886E+16)	(0.507)
0.2020E−03	1.600	3.000	−1.000	LINEAR	0.786
	(0.773)	(1.642)	(423.91)	(0.886E+16)	(0.507)
0.2059E−03	1.800	3.000	−1.000	SATURATION	0.775
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2087E−03	2.000	3.000	−1.000	SATURATION	0.764
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2112E−03	2.200	3.000	−1.000	SATURATION	0.754
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.2136E−03	2.400	3.000	−1.000	SATURATION	0.744
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2158E−03	2.600	3.000	−1.000	SATURATION	0.734
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2180E−03	2.800	3.000	−1.000	SATURATION	0.724
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2201E−03	3.000	3.000	−1.000	SATURATION	0.714
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2222E−03	3.200	3.000	−1.000	SATURATION	0.704
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2243E−03	3.400	3.000	−1.000	SATURATION	0.694
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2263E−03	3.600	3.000	−1.000	SATURATION	0.684
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2283E−03	3.800	3.000	−1.000	SATURATION	0.673
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2304E−03	4.000	3.000	−1.000	SATURATION	0.663
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2324E−03	4.200	3.000	−1.000	SATURATION	0.652
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2343E−03	4.400	3.000	−1.000	SATURATION	0.641
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2363E−03	4.600	3.000	−1.000	SATURATION	0.630
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2383E−03	4.800	3.000	−1.000	SATURATION	0.619
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.2403E−03	5.000	3.000	−1.000	SATURATION	0.608
	(0.773)	(1.642)	(421.91)	(0.886E+16)	(0.507)
0.0000E+00	0.000	4.000	−1.000	LINEAR	0.816
	(0.773)	(2.237)	(497.68)	(0.886E+16)	(0.507)
0.6654E−04	0.200	4.000	−1.000	LINEAR	0.812
	(0.773)	(2.245)	(482.64)	(0.886E+16)	(0.507)
0.1245E−03	0.400	4.000	−1.000	LINEAR	0.809
	(0.773)	(2.245)	(468.74)	(0.886E+16)	(0.507)
0.1749E−03	0.600	4.000	−1.000	LINEAR	0.805
	(0.773)	(2.245)	(455.86)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.2185E−03	0.800	4.000	−1.000	LINEAR	0.802
	(0.773)	(2.245)	(443.92)	(0.886E+16)	(0.507)
0.2558E−03	1.000	4.000	−1.000	LINEAR	0.798
	(0.773)	(2.245)	(432.83)	(0.886E+16)	(0.507)
0.2874E−03	1.200	4.000	−1.000	LINEAR	0.794
	(0.773)	(2.245)	(422.52)	(0.886E+16)	(0.507)
0.3137E−03	1.400	4.000	−1.000	LINEAR	0.790
	(0.773)	(2.245)	(412.92)	(0.886E+16)	(0.507)
0.3353E−03	1.600	4.000	−1.000	LINEAR	0.786
	(0.773)	(2.245)	(403.97)	(0.886E+16)	(0.507)
0.3525E−03	1.800	4.000	−1.000	LINEAR	0.781
	(0.773)	(2.245)	(395.62)	(0.886E+16)	(0.507)
0.3655E−03	2.000	4.000	−1.000	LINEAR	0.777
	(0.773)	(2.245)	(387.83)	(0.886E+16)	(0.507)
0.3747E−03	2.200	4.000	−1.000	LINEAR	0.773
	(0.773)	(2.245)	(380.54)	(0.886E+16)	(0.507)
0.3801E−03	2.400	4.000	−1.000	SATURATION	0.763
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.3837E−03	2.600	4.000	−1.000	SATURATION	0.754
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.3868E−03	2.800	4.000	−1.000	SATURATION	0.745
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.3897E−03	3.000	4.000	−1.000	SATURATION	0.737
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.3926E−03	3.200	4.000	−1.000	SATURATION	0.728
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.3953E−03	3.400	4.000	−1.000	SATURATION	0.720
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.3979E−03	3.600	4.000	−1.000	SATURATION	0.711
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.4005E−03	3.800	4.000	−1.000	SATURATION	0.702
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.4031E−03	4.000	4.000	−1.000	SATURATION	0.693
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.4056E−03	4.200	4.000	−1.000	SATURATION	0.685
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.4082E−03	4.400	4.000	−1.000	SATURATION	0.676
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.4106E−03	4.600	4.000	−1.000	SATURATION	0.666
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.4131E−03	4.800	4.000	−1.000	SATURATION	0.657
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.4156E−03	5.000	4.000	−1.000	SATURATION	0.648
	(0.773)	(2.245)	(378.96)	(0.886E+16)	(0.507)
0.0000E+00	0.000	5.000	−1.000	LINEAR	0.816
	(0.773)	(2.789)	(470.42)	(0.886E+16)	(0.507)
0.8320E−04	0.200	5.000	−1.000	LINEAR	0.812
	(0.773)	(2.797)	(456.96)	(0.886E+16)	(0.507)
0.1574E−03	0.400	5.000	−1.000	LINEAR	0.809
	(0.773)	(2.797)	(444.48)	(0.886E+16)	(0.507)
0.2235E−03	0.600	5.000	−1.000	LINEAR	0.805
	(0.773)	(2.797)	(432.89)	(0.886E+16)	(0.507)
0.2824E−03	0.800	5.000	−1.000	LINEAR	0.802
	(0.773)	(2.797)	(422.10)	(0.886E+16)	(0.507)
0.3346E−03	1.000	5.000	−1.000	LINEAR	0.798
	(0.773)	(2.797)	(412.07)	(0.886E+16)	(0.507)
0.3807E−03	1.200	5.000	−1.000	LINEAR	0.794
	(0.773)	(2.797)	(402.71)	(0.886E+16)	(0.507)
0.4213E−03	1.400	5.000	−1.000	LINEAR	0.790
	(0.773)	(2.797)	(393.98)	(0.886E+16)	(0.507)
0.4567E−03	1.600	5.000	−1.000	LINEAR	0.786
	(0.773)	(2.797)	(385.83)	(0.886E+16)	(0.507)
0.4874E−03	1.800	5.000	−1.000	LINEAR	0.781
	(0.773)	(2.797)	(378.20)	(0.886E+16)	(0.507)
0.5138E−03	2.000	5.000	−1.000	LINEAR	0.777
	(0.773)	(2.797)	(371.07)	(0.886E+16)	(0.507)
0.5360E−03	2.200	5.000	−1.000	LINEAR	0.773
	(0.773)	(2.797)	(364.39)	(0.886E+16)	(0.507)
0.5544E−03	2.400	5.000	−1.000	LINEAR	0.768
	(0.773)	(2.797)	(358.13)	(0.886E+16)	(0.507)
0.5693E−03	2.600	5.000	−1.000	LINEAR	0.764
	(0.773)	(2.797)	(352.27)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.5808E−03	2.800	5.000	−1.000	SATURATION	0.759
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.5861E−03	3.000	5.000	−1.000	SATURATION	0.750
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.5899E−03	3.200	5.000	−1.000	SATURATION	0.742
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.5934E−03	3.400	5.000	−1.000	SATURATION	0.734
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.5967E−03	3.600	5.000	−1.000	SATURATION	0.726
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.5998E−03	3.800	5.000	−1.000	SATURATION	0.718
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.6029E−03	4.000	5.000	−1.000	SATURATION	0.710
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.6059E−03	4.200	5.000	−1.000	SATURATION	0.702
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.6088E−03	4.400	5.000	−1.000	SATURATION	0.694
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.6116E−03	4.600	5.000	−1.000	SATURATION	0.686
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.6145E−03	4.800	5.000	−1.000	SATURATION	0.678
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)
0.6173E−03	5.000	5.000	−1.000	SATURATION	0.670
	(0.773)	(2.797)	(346.85)	(0.886E+16)	(0.507)

4. Example 2, Line Printer Listing for I_d Versus L

T1. PROCESSING PARAMETER INPUTS FOR CHARGE-SHARING MODEL

W → 5.0	NII → 3.E16	VFB0 → −0.9
WR → 1.2	XII → 0.05	TEMP → 300.
L → 2.5	NSUB → 1.E15	RHO → 20.
TOX → 300.0	XSUB → 0.43	RCONT → 50.
XJ → 0.4		
DELXJ → 0.65		
LS → 10.5		
LD → 10.5		

UNITS:

TOX → Angstroms	RHO → Ohms/Square
NII → cm-3	RCONT → Ohms
NSUB → cm-3	DELXJ → Unitless
VFB0 → Volts	
TEMP → Kelvin	ALL OTHERS → Microns

T2. TERMINAL AND VOLTAGE ASSIGNMENTS FOR CHARGE-SHARING MODEL

Axes Assignment	Low	High	Step	UNDEF Terminal
XAXIS → L	2.0	5.0	0.5	FIXVAR → VDD
FAMILY → VGG	0.0	5.0	1.0	FIXVAL → 2.5
PRMTAR → VBB	−1.0	0.0	−1.0	
REFVAR → VSS	0.0	0.0	0.0	

NOTES: The axes assignments can be the four terminals VDD, VGG, VBB, VSS or one of the terminals can be replaced by an input processing parameter from the previous menu. If one of the axes assignments is an input processing parameter, then one device terminal must be defined in the undefined terminal section by name = FIXVAR and by value = FIXVAL.

T3. CONTROL PARAMETERS FOR CHARGE-SHARING MODEL

FUNCTN → 1	→ numeric field	CRT → 0 0 = no
VALUE1 →	← alpha field	PRINTR → 1 1 = yes
VALUE2 →	← alpha field	
VALUE3 →	← numeric field	OUTPUT FILE → DATAXX::31

Function #	Function Description
1	Plot Id on the Y-axis
2	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Percent Delta of VALUE2
3	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Actual Delta of VALUE2

COMPUTED VALUES

WEFF = 3.800	COX = 0.12E-06	VKT = 0.02586
LEFF = 1.480	RS = 92.00	NI = 0.15E+11
RJ = 0.260	RD = 81.30	TWOPF = 0.77254

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.1029E−11	2.000	0.000	0.000	SUB−VT	0.795
	(0.484)	(0.000)	(691.02)	(0.233E+17)	(0.205)
0.3586E−12	2.500	0.000	0.000	SUB−VT	0.847
	(0.506)	(0.000)	(427.58)	(0.233E+17)	(0.205)
0.1854E−12	3.000	0.000	0.000	SUB−VT	0.877
	(0.520)	(0.000)	(440.45)	(0.233E+17)	(0.205)
0.1165E−12	3.500	0.000	0.000	SUB−VT	0.897
	(0.529)	(0.000)	(454.97)	(0.233E+17)	(0.205)
0.8197E−13	4.000	0.000	0.000	SUB−VT	0.912
	(0.535)	(0.000)	(468.57)	(0.233E+17)	(0.205)
0.6197E−13	4.500	0.000	0.000	SUB−VT	0.923
	(0.540)	(0.000)	(480.74)	(0.233E+17)	(0.205)
0.4922E−13	5.000	0.000	0.000	SUB−VT	0.931
	(0.544)	(0.000)	(491.49)	(0.233E+17)	(0.205)
0.1980E−04	2.000	1.000	0.000	SATURATION	0.721
	(0.484)	(0.353)	(528.10)	(0.233E+17)	(0.205)
0.1294E−04	2.500	1.000	0.000	SATURATION	0.802
	(0.506)	(0.344)	(543.42)	(0.233E+17)	(0.205)
0.9533E−05	3.000	1.000	0.000	SATURATION	0.847
	(0.520)	(0.336)	(554.21)	(0.233E+17)	(0.205)
0.7518E−05	3.500	1.000	0.000	SATURATION	0.875
	(0.529)	(0.329)	(561.91)	(0.233E+17)	(0.205)
0.6198E−05	4.000	1.000	0.000	SATURATION	0.894
	(0.535)	(0.332)	(567.16)	(0.233E+17)	(0.205)
0.5264E−05	4.500	1.000	0.000	SATURATION	0.908
	(0.540)	(0.328)	(571.65)	(0.233E+17)	(0.205)
0.4572E−05	5.000	1.000	0.000	SATURATION	0.919
	(0.544)	(0.326)	(575.24)	(0.233E+17)	(0.205)
0.1301E−03	2.000	2.000	0.000	SATURATION	0.746
	(0.484)	(0.968)	(436.78)	(0.233E+17)	(0.205)
0.9521E−04	2.500	2.000	0.000	SATURATION	0.815
	(0.506)	(0.992)	(456.78)	(0.233E+17)	(0.205)
0.7528E−04	3.000	2.000	0.000	SATURATION	0.855
	(0.520)	(1.002)	(472.66)	(0.233E+17)	(0.205)
0.6236E−04	3.500	2.000	0.000	SATURATION	0.880
	(0.529)	(1.008)	(485.01)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.5329E−04	4.000	2.000	0.000	SATURATION	0.898
	(0.535)	(1.013)	(494.87)	(0.233E+17)	(0.205)
0.4655E−04	4.500	2.000	0.000	SATURATION	0.911
	(0.540)	(1.017)	(502.89)	(0.233E+17)	(0.205)
0.4134E−04	5.000	2.000	0.000	SATURATION	0.921
	(0.544)	(1.020)	(509.54)	(0.233E+17)	(0.205)
0.2868E−03	2.000	3.000	0.000	SATURATION	0.769
	(0.484)	(1.517)	(379.04)	(0.233E+17)	(0.205)
0.2196E−03	2.500	3.000	0.000	SATURATION	0.830
	(0.506)	(1.578)	(399.32)	(0.233E+17)	(0.205)
0.1792E−03	3.000	3.000	0.000	SATURATION	0.865
	(0.520)	(1.615)	(416.12)	(0.233E+17)	(0.205)
0.1519E−03	3.500	3.000	0.000	SATURATION	0.888
	(0.529)	(1.644)	(429.79)	(0.233E+17)	(0.205)
0.1321E−03	4.000	3.000	0.000	SATURATION	0.904
	(0.535)	(1.666)	(441.09)	(0.233E+17)	(0.205)
0.1170E−03	4.500	3.000	0.000	SATURATION	0.916
	(0.540)	(1.683)	(450.54)	(0.233E+17)	(0.205)
0.1050E−03	5.000	3.000	0.000	SATURATION	0.925
	(0.544)	(1.698)	(458.57)	(0.233E+17)	(0.205)
0.4727E−03	2.000	4.000	0.000	SATURATION	0.784
	(0.484)	(2.013)	(338.71)	(0.233E+17)	(0.205)
0.3700E−03	2.500	4.000	0.000	SATURATION	0.840
	(0.506)	(2.113)	(357.94)	(0.233E+17)	(0.205)
0.3070E−03	3.000	4.000	0.000	SATURATION	0.873
	(0.520)	(2.184)	(374.33)	(0.233E+17)	(0.205)
0.2636E−03	3.500	4.000	0.000	SATURATION	0.894
	(0.529)	(2.238)	(388.09)	(0.233E+17)	(0.205)
0.2317E−03	4.000	4.000	0.000	SATURATION	0.910
	(0.535)	(2.327)	(398.13)	(0.233E+17)	(0.205)
0.2069E−03	4.500	4.000	0.000	SATURATION	0.921
	(0.540)	(2.362)	(408.15)	(0.233E+17)	(0.205)
0.1872E−03	5.000	4.000	0.000	SATURATION	0.930
	(0.544)	(2.391)	(416.81)	(0.233E+17)	(0.205)
0.6802E−03	2.000	5.000	0.000	LINEAR	0.795
	(0.484)	(2.520)	(307.60)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.5355E−03	2.500	5.000	0.000	LINEAR	0.847
	(0.506)	(2.661)	(330.00)	(0.233E+17)	(0.205)
0.4470E−03	3.000	5.000	0.000	LINEAR	0.877
	(0.520)	(2.767)	(348.90)	(0.233E+17)	(0.205)
0.3858E−03	3.500	5.000	0.000	LINEAR	0.897
	(0.529)	(2.849)	(364.56)	(0.233E+17)	(0.205)
0.3404E−03	4.000	5.000	0.000	LINEAR	0.912
	(0.535)	(2.914)	(377.63)	(0.233E+17)	(0.205)
0.3051E−03	4.500	5.000	0.000	LINEAR	0.923
	(0.540)	(2.968)	(388.64)	(0.233E+17)	(0.205)
0.2767E−03	5.000	5.000	0.000	LINEAR	0.931
	(0.544)	(3.013)	(398.03)	(0.233E+17)	(0.205)
0.2093E−16	2.000	0.000	−1.000	SUB−VT	0.684
	(0.737)	(3.013)	(332.76)	(0.886E+16)	(0.507)
0.2962E−17	2.500	0.000	−1.000	SUB−VT	0.766
	(0.773)	(3.013)	(481.08)	(0.886E+16)	(0.507)
0.9423E−18	3.000	0.000	−1.000	SUB−VT	0.814
	(0.796)	(3.013)	(477.91)	(0.886E+16)	(0.507)
0.4361E−18	3.500	0.000	−1.000	SUB−VT	0.845
	(0.811)	(3.013)	(484.35)	(0.886E+16)	(0.507)
0.2485E−18	4.000	0.000	−1.000	SUB−VT	0.868
	(0.821)	(3.013)	(493.19)	(0.886E+16)	(0.507)
0.1610E−18	4.500	0.000	−1.000	SUB−VT	0.884
	(0.829)	(3.013)	(502.28)	(0.886E+16)	(0.507)
0.1136E−18	5.000	0.000	−1.000	SUB−VT	0.897
	(0.836)	(3.013)	(510.91)	(0.886E+16)	(0.507)
0.7853E−05	2.000	1.000	−1.000	SATURATION	0.480
	(0.737)	(0.275)	(565.07)	(0.886E+16)	(0.507)
0.4012E−05	2.500	1.000	−1.000	SATURATION	0.649
	(0.773)	(0.196)	(580.89)	(0.886E+16)	(0.507)
0.2462E−05	3.000	1.000	−1.000	SATURATION	0.736
	(0.796)	(0.177)	(588.00)	(0.886E+16)	(0.507)
0.1703E−05	3.500	1.000	−1.000	SATURATION	0.788
	(0.811)	(0.164)	(592.93)	(0.886E+16)	(0.507)
0.1270E−05	4.000	1.000	−1.000	SATURATION	0.823
	(0.821)	(0.154)	(596.53)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.9969E−06	4.500	1.000	−1.000	SATURATION	0.848
	(0.829)	(0.147)	(599.27)	(0.886E+16)	(0.507)
0.8123E−06	5.000	1.000	−1.000	SATURATION	0.866
	(0.836)	(0.142)	(601.40)	(0.886E+16)	(0.507)
0.1185E−03	2.000	2.000	−1.000	SATURATION	0.585
	(0.737)	(0.961)	(470.50)	(0.886E+16)	(0.507)
0.8253E−04	2.500	2.000	−1.000	SATURATION	0.701
	(0.773)	(0.970)	(483.33)	(0.886E+16)	(0.507)
0.6327E−04	3.000	2.000	−1.000	SATURATION	0.767
	(0.796)	(0.969)	(495.32)	(0.886E+16)	(0.507)
0.5131E−04	3.500	2.000	−1.000	SATURATION	0.809
	(0.811)	(0.968)	(505.27)	(0.886E+16)	(0.507)
0.4316E−04	4.000	2.000	−1.000	SATURATION	0.838
	(0.821)	(0.967)	(513.49)	(0.886E+16)	(0.507)
0.3725E−04	4.500	2.000	−1.000	SATURATION	0.859
	(0.829)	(0.967)	(520.34)	(0.886E+16)	(0.507)
0.3277E−04	5.000	2.000	−1.000	SATURATION	0.875
	(0.836)	(0.966)	(526.11)	(0.886E+16)	(0.507)
0.2911E−03	2.000	3.000	−1.000	SATURATION	0.645
	(0.737)	(1.591)	(410.23)	(0.886E+16)	(0.507)
0.2147E−03	2.500	3.000	−1.000	SATURATION	0.739
	(0.773)	(1.642)	(421.94)	(0.886E+16)	(0.507)
0.1715E−03	3.000	3.000	−1.000	SATURATION	0.793
	(0.796)	(1.671)	(434.29)	(0.886E+16)	(0.507)
0.1435E−03	3.500	3.000	−1.000	SATURATION	0.829
	(0.811)	(1.693)	(445.36)	(0.886E+16)	(0.507)
0.1237E−03	4.000	3.000	−1.000	SATURATION	0.854
	(0.821)	(1.710)	(454.98)	(0.886E+16)	(0.507)
0.1088E−03	4.500	3.000	−1.000	SATURATION	0.872
	(0.829)	(1.724)	(463.31)	(0.886E+16)	(0.507)
0.9728E−04	5.000	3.000	−1.000	SATURATION	0.887
	(0.836)	(1.735)	(470.54)	(0.886E+16)	(0.507)
0.5075E−03	2.000	4.000	−1.000	SATURATION	0.671
	(0.737)	(2.150)	(369.35)	(0.886E+16)	(0.507)
0.3820E−03	2.500	4.000	−1.000	SATURATION	0.759
	(0.773)	(2.244)	(379.00)	(0.886E+16)	(0.507)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
0.3102E−03	3.000	4.000	−1.000	SATURATION	0.809
	(0.796)	(2.309)	(390.48)	(0.886E+16)	(0.507)
0.2630E−03	3.500	4.000	−1.000	SATURATION	0.842
	(0.811)	(2.359)	(401.37)	(0.886E+16)	(0.507)
0.2292E−03	4.000	4.000	−1.000	SATURATION	0.866
	(0.821)	(2.398)	(411.18)	(0.886E+16)	(0.507)
0.2035E−03	4.500	4.000	−1.000	SATURATION	0.883
	(0.829)	(2.430)	(419.90)	(0.886E+16)	(0.507)
0.1833E−03	5.000	4.000	−1.000	SATURATION	0.896
	(0.836)	(2.456)	(427.63)	(0.886E+16)	(0.507)
0.7437E−03	2.000	5.000	−1.000	LINEAR	0.684
	(0.737)	(2.657)	(343.11)	(0.886E+16)	(0.507)
0.5623E−03	2.500	5.000	−1.000	LINEAR	0.766
	(0.773)	(2.795)	(355.15)	(0.886E+16)	(0.507)
0.4597E−03	3.000	5.000	−1.000	LINEAR	0.814
	(0.796)	(2.897)	(368.67)	(0.886E+16)	(0.507)
0.3919E−03	3.500	5.000	−1.000	LINEAR	0.845
	(0.811)	(2.977)	(381.11)	(0.886E+16)	(0.507)
0.3430E−03	4.000	5.000	−1.000	LINEAR	0.868
	(0.821)	(3.041)	(392.06)	(0.886E+16)	(0.507)
0.3057E−03	4.500	5.000	−1.000	LINEAR	0.884
	(0.829)	(3.093)	(401.61)	(0.886E+16)	(0.507)
0.2762E−03	5.000	5.000	−1.000	LINEAR	0.897
	(0.836)	(3.137)	(409.94)	(0.886E+16)	(0.507)

5. EXAMPLE 3, Line Printer Listing of $d(I_d)/d(L)$ Versus T_{ox}

T1. PROCESSING PARAMETER INPUTS FOR CHARGE-SHARING MODEL

W → 5.0	NII → 3.E16	VFB0 → −0.9
WR → 1.2	XII → 0.05	TEMP → 300.0
L → 2.5	NSUB → 1.E15	RHO → 20.0
TOX → 300.0	XSUB → 0.43	RCONT → 50.0
XJ → 0.4		
DELXJ → 0.65		
LS → 10.5		
LD → 1.5		

UNITS:

TOX → Angstroms	RHO → Ohms/Square
NII → cm-3	RCONT → Ohms
NSUB → cm-3	DELXJ → Unitless
VFB0 → Volts	
TEMP → Kelvin	ALL OTHERS → Microns

T2. TERMINAL AND VOLTAGE ASSIGNMENTS FOR CHARGE-SHARING MODEL

Axes Assignment	Low	High	Step	UNDEF Terminal
XAXIS → TOX	250.0	500.0	25.0	FIXVAR → VDD
FAMILY → VGG	0.0	5.0	1.0	FIXVAL → 2.5
PRMTAR → VBB	0.0	0.0	−1.0	
REFVAR → VSS	0.0	0.0	0.0	

NOTES: The axes assignments can be the four terminals VDD, VGG, VBB, VSS or one of the terminals can be replaced by an input processing parameter from the previous menu. If one of the axes assignments is an input processing parameter, then one device terminal must be defined in the undefined terminal section by name = FIXVAR and by value = FIXVAL.

T3. CONTROL PARAMETERS FOR CHARGE-SHARING MODEL

FUNCTN → 2	← numeric field	CRT → 0 0 = no
VALUE1 →	← alpha field	PRINTR → 1 1 = yes
VALUE2 → L	← alpha field	
VALUE3 → 0.5	← numeric field	OUTPUT FILE → DATAXX::31

Function #	Function Description
1	Plot Id on the Y-axis
2	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Percent Delta of VALUE2
3	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Actual Delta of VALUE2

COMPUTED VALUES

WEFF = 3.800	COX = 0.14E-06	VKT = 0.02586
LEFF = 1.993	RS = 92.00	NI = 0.15E+11
RJ = 0.260	RD = 92.00	TWOPF = 0.75100

FUNCTN # 2	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
−0.4540E−11	250.000	0.000	0.000	SUB−VT	0.849
	(0.399)	(0.000)	(408.47)	(.233E+17)	(0.205)
−0.1566E−11	275.000	0.000	0.000	SUB−VT	0.847
	(0.452)	(0.000)	(407.77)	(0.233E+17)	(0.205)
−0.5784E−12	300.000	0.000	0.000	SUB−VT	0.846
	(0.506)	(0.000)	(407.19)	(0.233E+17)	(0.205)
−0.2275E−12	325.000	0.000	0.000	SUB−VT	0.844
	(0.559)	(0.000)	(406.71)	(0.233E+17)	(0.205)
−0.9499E−13	350.000	0.000	0.000	SUB−VT	842
	(0.612)	(0.000)	(406.29)	(0.233E+17)	(0.205)
−0.4194E−13	375.000	0.000	0.000	SUB−VT	840
	(0.665)	(0.000)	(405.94)	(0.233E+17)	(0.205)
−0.1952E−13	400.000	0.000	0.000	SUB- VT	839
	(0.718)	(0.000)	(405.63)	(0.233E+17)	(0.205)
−0.9541E−14	425.000	0.000	0.000	SUB−VT	837
	(0.770)	(0.000)	(405.35)	(0.233E+17)	(0.205)
−0.4883E−14	450.000	0.000	0.000	SUB−VT	836
	(0.823)	(0.000)	(405.10)	(0.233E+17)	(0.205)
−0.2609E−14	475.000	0.000	0.000	SUB−VT	834
	(0.875)	(0.000)	(404.88)	(0.233E+17)	(0.205)
−0.1451E−14	500.000	0.000	0.000	SUB−VT	832
	(0.927)	(0.000)	(404.68)	(0.233E+17)	(0.205)
−0.1557E−04	250.000	1.000	0.000	SATURATION	807
	(0.399)	(0.438)	(532.38)	(0.233E+17)	(0.205)
−0.1175E−04	275.000	1.000	0.000	SATURATION	804
	(0.452)	(0.390)	(537.86)	(0.233E+17)	(0.205)
−0.9108E−05	300.000	1.000	0.000	SATURATION	801
	(0.506)	(0.345)	(543.11)	(0.233E+17)	(0.205)
−0.7024E−05	325.000	1.000	0.000	SATURATION	798
	(0.559)	(0.308)	(547.31)	(0.233E+17)	(0.205)
−0.5318E−05	350.000	1.000	0.000	SATURATION	796
	(0.612)	(0.267)	(551.92)	(0.233E+17)	(0.205)
−0.3928E−05	375.000	1.000	0.000	SATURATION	793
	(0.665)	(0.223)	(556.88)	(0.233E+17)	(0.205)
−0.2834E−05	400.000	1.000	0.000	SATURATION	791
	(0.718)	(0.184)	(561.25)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
−0.1980E−05	425.000	1.000	0.000	SATURATION	789
	(0.770)	(0.150)	(565.03)	(0.233E+17)	(0.205)
−0.1304E−05	450.000	1.000	0.000	SATURATION	787
	(0.823)	(0.114)	(568.96)	(0.233E+17)	(0.205)
−0.7844E−06	475.000	1.000	0.000	SATURATION	784
	(0.875)	(0.079)	(572.88)	(0.233E+17)	(0.205)
−0.3999E−06	500.000	1.000	0.000	SATURATION	782
	(0.927)	(0.044)	(576.65)	(0.233E+17)	(0.205)
−0.7310E−04	250.000	2.000	0.000	SATURATION	821
	(0.399)	(1.122)	(445.06)	(0.233E+17)	(0.205)
−0.5775E−04	275.000	2.000	0.000	SATURATION	818
	(0.452)	(1.046)	(451.51)	(0.233E+17)	(0.205)
−0.5064E−04	300.000	2.000	0.000	SATURATION	814
	(0.506)	(0.993)	(456.30)	(0.233E+17)	(0.205)
−0.4450E−04	325.000	2.000	0.000	SATURATION	811
	(0.559)	(0.940)	(460.92)	(0.233E+17)	(0.205)
−0.3920E−04	350.000	2.000	0.000	SATURATION	808
	(0.612)	(0.889)	(465.39)	(0.233E+17)	(0.205)
−0.3475E−04	375.000	2.000	0.000	SATURATION	805
	(0.665)	(0.856)	(468.38)	(0.233E+17)	(0.205)
−0.3069E−04	400.000	2.000	0.000	SATURATION	802
	(0.718)	(0.812)	(472.23)	(0.233E+17)	(0.205)
−0.2714E−04	425.000	2.000	0.000	SATURATION	799
	(0.770)	(0.769)	(475.91)	(0.233E+17)	(0.205)
−0.2400E−04	450.000	2.000	0.000	SATURATION	796
	(0.823)	(0.728)	(479.43)	(0.233E+17)	(0.205)
−0.2107E−04	475.000	2.000	0.000	SATURATION	794
	(0.875)	(0.672)	(484.19)	(0.233E+17)	(0.205)
−0.1860E−04	500.000	2.000	0.000	SATURATION	791
	(0.927)	(0.630)	(487.81)	(0.233E+17)	(0.205)
−0.1302E−03	250.000	3.000	0.000	SATURATION	836
	(0.399)	(1.724)	(388.58)	(0.233E+17)	(0.205)
−0.1125E−03	275.000	3.000	0.000	SATURATION	832
	(0.452)	(1.670)	(392.76)	(0.233E+17)	(0.205)
−0.1003E−03	300.000	3.000	0.000	SATURATION	828
	(0.506)	(1.577)	(398.80)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
−0.9064E−04	325.000	3.000	0.000	SATURATION	825
	(0.559)	(1.520)	(402.97)	(0.233E+17)	(0.205)
−0.8212E−04	350.000	3.000	0.000	SATURATION	822
	(0.612)	(1.463)	(406.99)	(0.233E+17)	(0.205)
−0.7466E−04	375.000	3.000	0.000	SATURATION	819
	(0.665)	(1.408)	(410.89)	(0.233E+17)	(0.205)
−0.6808E−04	400.000	3.000	0.000	SATURATION	815
	(0.718)	(1.353)	(414.69)	(0.233E+17)	(0.205)
−0.6264E−04	425.000	3.000	0.000	SATURATION	813
	(0.770)	(1.327)	(416.78)	(0.233E+17)	(0.205)
−0.5737E−04	450.000	3.000	0.000	SATURATION	809
	(0.823)	(1.281)	(420.02)	(0.233E+17)	(0.205)
−0.5271E−04	475.000	3.000	0.000	SATURATION	807
	(0.875)	(1.236)	(423.12)	(0.233E+17)	(0.205)
−0.4850E−04	500.000	3.000	0.000	SATURATION	804
	(0.927)	(1.193)	(426.10)	(0.233E+17)	(0.205)
−0.1991E−03	250.000	4.000	0.000	SATURATION	845
	(0.399)	(2.272)	(348.05)	(0.233E+17)	(0.205)
−0.1727E−03	275.000	4.000	0.000	SATURATION	842
	(0.452)	(2.214)	(351.95)	(0.233E+17)	(0.205)
−0.1549E−03	300.000	4.000	0.000	SATURATION	839
	(0.506)	(2.113)	(357.42)	(0.233E+17)	(0.205)
−0.1412E−03	325.000	4.000	0.000	SATURATION	836
	(0.559)	(2.051)	(361.24)	(0.233E+17)	(0.205)
−0.1290E−03	350.000	4.000	0.000	SATURATION	833
	(0.612)	(1.990)	(364.90)	(0.233E+17)	(0.205)
−0.1184E−03	375.000	4.000	0.000	SATURATION	830
	(0.665)	(1.930)	(368.44)	(0.233E+17)	(0.205)
−0.1091E−03	400.000	4.000	0.000	SATURATION	.827
	(0.718)	(1.871)	(371.87)	(0.233E+17)	(0.205)
−0.1007E−03	425.000	4.000	0.000	SATURATION	824
	(0.770)	(1.814)	(375.22)	(0.233E+17)	(0.205)
−0.9332E−04	450.000	4.000	0.000	SATURATION	821
	(0.823)	(1.757)	(378.49)	(0.233E+17)	(0.205)
−0.8743E−04	475.000	4.000	0.000	SATURATION	819
	(0.875)	(1.740)	(379.85)	(0.233E+17)	(0.205)

FUNCTN # 1	XAX (VT)	FAM (VDSAT)	PRM (MU)	REGION (NA)	F (XDEPLT)
−0.8126E−04	500.000	4.000	0.000	SATURATION	816
	(0.927)	(1.693)	(382.61)	(0.233E+17)	(0.205)
−0.2649E−03	250.000	5.000	0.000	LINEAR	849
	(0.399)	(2.779)	(325.91)	(0.233E+17)	(0.205)
−0.2397E−03	275.000	5.000	0.000	LINNEAR	847
	(0.452)	(2.719)	(327.85)	(0.233E+17)	(0.205)
−0.2182E−03	300.000	5.000	0.000	LINEAR	846
	(0.506)	(2.660)	(329.48)	(0.233E+17)	(0.205)
−0.1997E−03	325.000	5.000	0.000	LINEAR	844
	(0.559)	(2.543)	(330.88)	(0.233E+17)	(0.205)
−0.1827E−03	350.000	5.000	0.000	SATURATION	842
	(0.612)	(2.479)	(332.81)	(0.233E+17)	(0.205)
−0.1667E−03	375.000	5.000	0.000	SATURATION	839
	(0.665)	(2.415)	(336.07)	(0.233E+17)	(0.205)
−0.1539E−03	400.000	5.000	0.000	SATURATION	836
	(0.718)	(2.353)	(339.21)	(0.233E+17)	(0.205)
−0.1427E−03	425.000	5.000	0.000	SATURATION	833
	(0.770)	(2.292)	(342.27)	(0.233E+17)	(0.205)
−0.1328E−03	450.000	5.000	0.000	SATURATION	830
	(0.823)	(2.232)	(345.25)	(0.233E+17)	(0.205)
−0.1239E−03	475.000	5.000	0.000	SATURATION	828
	(0.875)	(2.172)	(348.16)	(0.233E+17)	(0.205)
−0.1171E−03	500.000	5.000	0.000	SATURATION	826
	(0.927)	(2.158)	(349.31)	(0.233E+17)	(0.205)

III. DESCRIPTION OF PROGRAM FLOW

The main for the program, ANDQSHR, defines COMMON and calls the two segments ANDQSHR1 and ANDQSHR2. See Figure H–2.

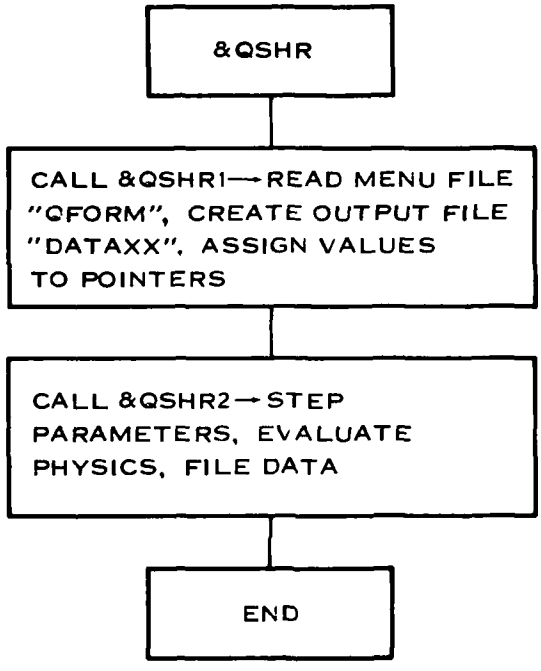


Figure H-2. Main Program and Segment Flow Diagram

The main for segment 1, ANDQSHR1, handles I/O processing and sets up a pointer system for indirect addressing of variables that are to be stepped (Figure H–3).

The main for segment 2, ANDQSHR2, steps parameters, evaluates physics for a given function selection, and files the data (Figure H–4).

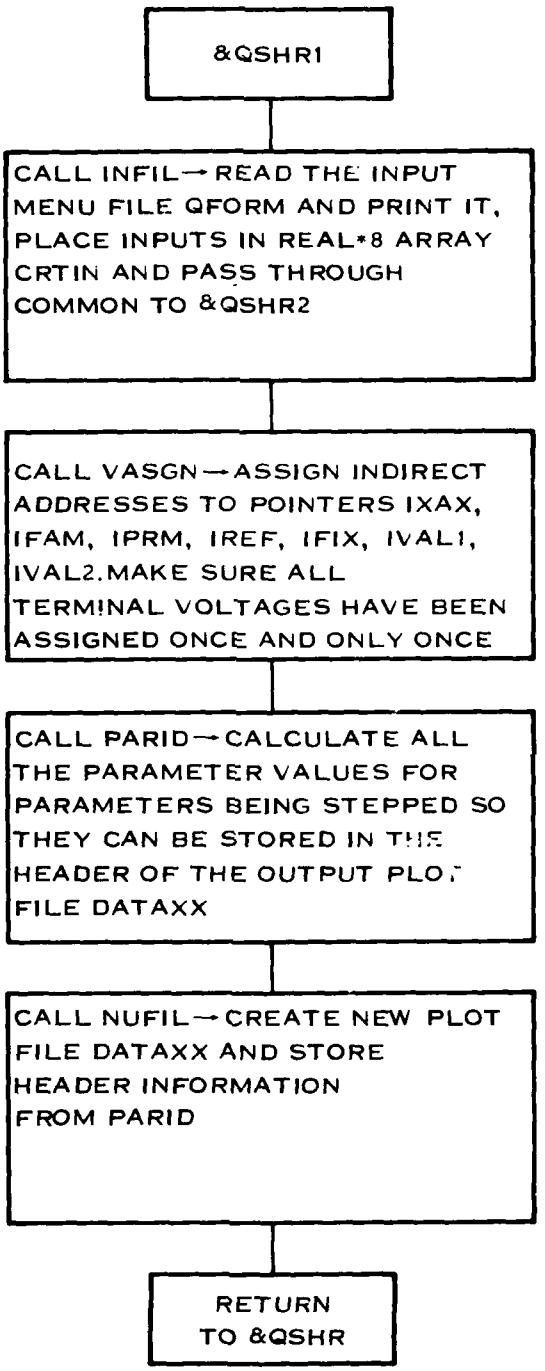


Figure H-3. Segment 1 Flow Diagram

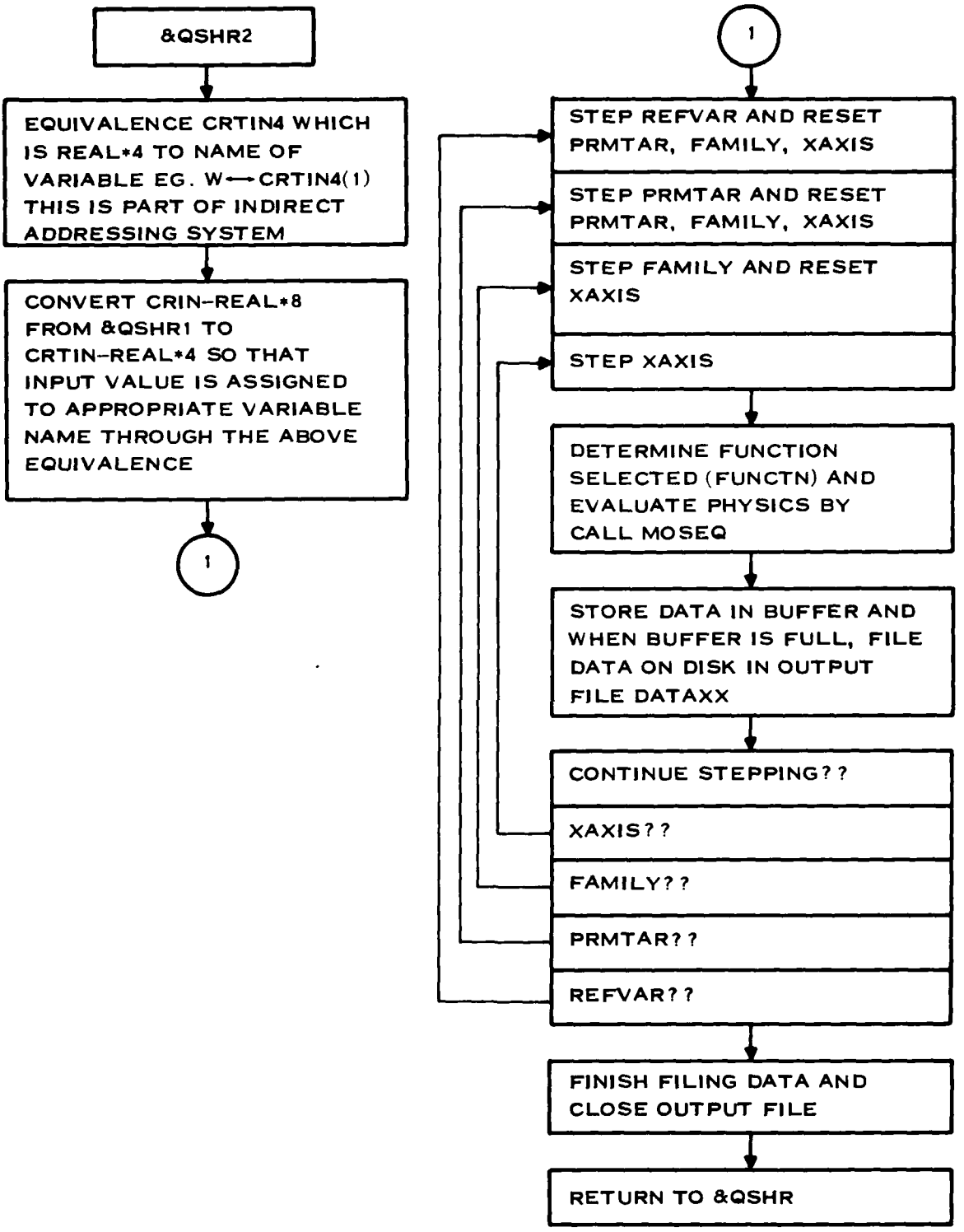


Figure H-4. Segment 2 Flow Diagram

IV. CHANGING THE PROGRAM

1. Adding Additional Input Parameters

The first screen of the input menu QFORM contains the processing parameter inputs. This section describes what must be done to add more inputs.

The input variables are stored in CRTIN(I)−REAL*8 and later in CRTIN4(I)-REAL*4. You must determine the value of "I" where you wish to store the input. The present assignments can be determined from the equivalences at the beginning of &QSHR2. Any "I" for an equivalence to a POOL−−can be used since the POOL−−are dummy variables. There are also places where part of the equivalence line has been commented out with "!." These values of "I" can also be used. The selection of the value of "I" is arbitrary as long as that value is not already used. Equivalence CRTIN4(I) and the name of the input variable which will be used in the program code (this may be different from the name in QFORM).

In PROGRAM QSHR2 the CRTIN(I)−REAL*8 are converted to CRTIN4(I)−REAL*4. Make sure the new variable is converted.

The new variable must be passed through the subroutine calls to MOSEQ. There are several places in PROGRAM QSHR2 where these calls occur and each call must have the new variable added. If the variable will have its value changed inside MOSEQ then you must make sure this changed value is not passed back from MOSEQ to QSHR2. For example:

```
PROGRAM QSHR2
  .
  .
CALL MOSEQ (W, . . .)
  .
  .
END
SUBROUTINE MOSEQ (W1, . . .)
  .
  .
W=W1*1.0E−4                          units conversion
  .                                  not passed back
  .
RETURN
```

The input variable must be added to the input menu file QFORM (screen one). Add the new variable mneumonic to one of the three columns in QFORM. The mneumonic does not have to be the same as the variable name in the equivalence statement of step 1. Be sure to leave the same number of spaces in QFORM for the new input value as are available for the old inputs or you will have problems.

Subroutine INFIL in &QSHR1 reads QFORM and puts the value in array CRTIN-REAL*8. Following the pattern in INFIL, be sure you read the entire line into IBUFF and then write the entire line to the terminal. Then use DECODE to put the value into CRTIN(I) where "I" is the number determined in step 1.

Subroutine VASGN in &QSHR1 determines if a variable is to be stepped. If it is, an index number is assigned to the pointer (IXAX, IFAM, IRPM, IREF, IFIX, IVAL1, IVAL2). The index number will have the value of "I" determined in step 1. Look for the section of code in VASGN where the number of characters moved is equal to the number of characters in the mneumonic name you used in QFORM

(must be six or less). Imitate the code in this section except the octal values assigned to IMATCH(J) represent the mneumonic name of the new variable, INDEX equals the value of "I" determined in step 1, and LABL(K) is assigned the hollerith of the mneumonic name on QFORM.

2. Adding New Functions

Screen three of the input menu QFORM allows the selection of different functions. This section describes what must be done to add more functions.

Near the end of subroutine VASGN-&QSHR1 is a section of code that looks for errors in function selection. This section makes sure that CRTIN4(26) lies within the range of valid function selection. If you are adding a new function, change the IF statement to reflect the larger number of available functions.

Screen three of the input menu QFORM has a comments section describing the function numbers. Add the new number and description to QFORM.

In program QSHR2−&QSHR2 is a section of code that determines the function selected and evaluates the physics in MOSEQ. The logic for the new function is added here by another ELSE IF to the IF-THEN-ELSE statement. Be sure that when you are finished with each function evaluation that all the CRTIN4(*) have the same values as when you started the function evaluation or you will have problems with stepping the changed CRTIN4(*). Study the implementations of the other functions in that section of code and follow their example.

Transfer Files

Compile Transfer File → /QSHRC

```
:RU,FTN4X,&QSHR::−31,,%QSHR::−31
:RU,FTN4X,&QSHR1::−31,,%QSHR1::−31
:RU,FTN4X,&QSHR2::−31,,%QSHR2::−31
:RU,FTN4X,&QSHR3::−31,,%QSHR3::−31
```

Loader Transfer File → /QSHRL and /QSHRM

/QSHRL

```
:OF,QSHR
:OF,QSHR1
:OF,QSHR2
:RU,LOADR,/QSHRM
:TR,−11
```

/QSHRM

```
OP,LB
RE,%QSHR::−31
RE,%QSHR1::−31
RE,%QSHR2::−31
RE,%QSHR3::−31
END
```

Run Transfer File → RUQSHR—assumes program SP'd.

```
:** THIS IS THE TRANSFER FILE TO RUN THE CHARGE-SHARING PROGRAM
:** IF ANY QUESTIONS CONTACT JOHN LEISS x 7901 Hillcrest
:SV,4,,IH
:DP, I am setting up the Charge-Sharing Program for you . . .
:RP,QSHR1
:RP,QSHR2
:SV,0
:RUN,QSHR
:SV,4,,IH
:DP, I am removing the Charge-Sharing Program from the system . . .
:OF,QSHR1
:OF,QSHR2
:DP, It's all gone now . . . thank you.
:SV,0
```

A listing of QFORM input menu file follows:

T1. PROCESSING PARAMETER INPUTS FOR CHARGE-SHARING MODEL

	N1 →	
W →	N2 →	MU0 →
WR →	N3 →	THETA0 →
L →	NSUB →	RHO →
TOX →	XSUB →	RCONT →
XJ →	X3 →	
DELXJ →	VFB0	
LS →	RH0 →	XUDSF →
LD →	RCONT →	VERROR →

UNITS:

TOX → Angstroms	RHO → Ohms/Square
NII → cm-3	RCONT → Ohms
NSUB → cm-3	DELXJ → Unitless
VFB0 → Volts	
TEMP → Kelvin	ALL OTHERS → Microns

T2. TERMINAL AND VOLTAGE ASSIGNMENTS FOR CHARGE-SHARING MODEL

Axes Assignment	Low	High	Step	UNDEF Terminal
XAXIS →				FIXVAR →
FAMILY →				FIXVAL →
PRMTAR →				
REFVAR →				

NOTES: The axes assignments can be the four terminals VDD, VGG, VBB, VSS or one of the terminals can be replaced by an input processing parameter, from the previous menu. If one of the axes assignments is an input processing parameter, then one device terminal must be defined in the undefined terminal section by name = FIXVAR and by value = FIXVAL.

T3. CONTROL PARAMETERS FOR CHARGE-SHARING MODEL

FUNCTN →	← numeric field	CRT → 0 0 = no
VALUE1 →	← alpha field	PRINTR → 1 1 = yes
VALUE2 →	← alpha field	
VALUE3 →	← numeric field	OUTPUT FILE →

Function #	Function Description
1	Plot Id on the Y-axis
2	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Percent Delta of VALUE2
3	Plot Partial(Id)/Partial(VALUE2) VALUE3 = Actual Delta of VALUE2

APPENDIX I

FITER USER'S MANUAL

I. INTRODUCTION

FITER is a general parameter extraction program that has been hardwired to fit the modified Shichman-Hodges MOS equation to experimentally measured I_D versus V_{DS}, V_{GS}, and V_{BS}.

FITER is written in Fortran (HP's FTN4X implementation), and runs on an HP 1000 mini-computer using the RTE-IVB operating system. This implementation of the program requires a 40-page partition (20 pages for code and 20 pages for EMA data space), to solve for up to 2,000 data points and 15 different parameters.

FITER uses two ASCII input files (menus) and one formatted data file. The calculated data output is stored in a formatted binary file that may be plotted by using the NPLOT program. The calculated parameter values may be output to the CRT device or the printer.

Parameters obtained from this program may be used in SPICE2 or MACMOS programs.

II. SYSTEM CONSIDERATIONS

The size of the program is 40 pages; however, if the program is to calculate parameters based on fewer than 2,000 data points, the load size may be decreased by decreasing the DIM statements for the CDATA EMA area.

The program FITER is a segmented program. The segments are FITER, FIN, FOUT, and PAFIT. FITER, FIN, and FOUT provide for system dependent functions (file and I/O manipulations) while the solution routines are contained in PAFIT.

An HP 1000 transfer file is included that will load the program and its segments and SP the program to a specified disk LU.

To load:

:TR,LODFIT

III. FITER OPERATION

FITER attempts to fit the model equation to the measured data by appropriate adjustment of the model parameters (staying within the restrictions defined by the user). The program uses a combination of the modified Gauss and the steepest descent methods to calculate parameter values. Using either an initial guess set by the user or computed by the program, I_D is calculated, and an error function is computed. The parameter values are then adjusted and the process is continued in an iterative manner to minimize the error function. When the convergence criteria are satisfied, the process terminates. At termination the program stores the calculated current in a newly created file, then outputs to the assigned IUNIT the user identification, program termination status, parameter names and values, number of iterations, and fit error.

IV. FITER EQUATIONS

FITER may fit to any equation as long as the number of parameters is less than 15. If user-defined equations are to be implemented, the user must modify MOSEQ to return the gradients and calculated values of the user defined equation.

This implementation of FITER utilizes a modified Shichman-Hodges MOS model equation:

```
PHIF = (K*T/Q) * LN(N/NI)
VT = VT0+BE*(SQRT(2PHIF-VBS)-SQRT(2*PHIF))-DE*(SQRT(VDS)) @ VBS<0
VGST = VGS - VT
VGVGST = ALPHA + GAMMA*VGST
VDSAT = VGST/AGVST
BETA = KP*(W-WR)/(L-TLD-LR)

FOR VGST<0
ID = 0

FOR VDSAT>VDS
ID = AGVGST*BETA*(2*VGST*VDS-AGVGST*VDS**2)/(1+THETA*VGST)

FOR VDSAT<VDS
ID = BETA*VGST**2*(1+LAMBDA*(ALPHA/AGVGST)**2*(VDS-VDSAT))/
     (1+THETA*VGST)
```

V. ERROR FUNCTION

Let pi denote the *i*th unknown model parameter, I_jM the *j*th measured current, and $I_j(pi)$ the *i*th calculated current obtained from the model equations.Then the error function is:

$$ERR = \sum_{j,IjM>=IMIN} (Ij - IjM / IjM) ** 2$$

where IMIN defines the smallest measured current that will be used for the parameter extraction.

VI. STARTING VALUES

The initial values for the parameters may either be assigned by the user or calculated by the program. If the user decides to have the program compute the initial values it will do so using the following simplified MOSFET equations:

```
ID = BETA*(VGS-VT)**2 /                    ;   VGS >= VT+VDS
     (1+THETA*VGST)
ID = BETA*(2*(VGS-VT)VDS-VDS**2) /         ;   VT+VDS>=VGS>=VT
     (1+THETA*VGST)
ID = 0                                     ;   VT>VGS

VT = VT0+BE*(SQRT(2*PHIF-VBS)-SQRT(2*PHIF))
```

The simplified equations are used to fit a selected subset of the current data points.

VII. PROGRAM TERMINATION

The program may terminate whenever:

1) The fit error is acceptable
2) The maximum number of iterations is exceeded.

The allowed number of iterations is set by the user in the control file.

The fit error is acceptable when:

At every iteration the error (ERRk+1) and the parameter change ($\lambda\Delta$ Pk+1) are calculated. If one of the following two conditions are met, then the process is considered converged.

1) |ERRk+1 − ERRk| <= RELTOL * max(|ERRk+1|,|ERRk|) + ABSTOL

2) |$\lambda\Delta$ Pk+1| <= RELTOL * max(1Pk+1|,|Pk|) + ABSTOL

where RELTOL and ABSTOL are the relative and absolute error tolerances—see Control File.

VIII. INPUT DATA FILE

If the data has been obtained using DTTMP (data acquisition program), the formatted binary file may be directly input to the FITER. Binary files produced by earlier versions of data acquisition programs (DTACK, DTACQ) are not formatted correctly, and will produce runtime and other miscellaneous errors. To use data taken by DTACK or DTACQ, first translate the data to ASCII using the program K2FIL, one of the utility programs available. The program will also accept an ASCII file. This manual will not attempt to describe the format of the binary file; however, a description of the ASCII file follows.

The ASCII file must be formatted in 80-columns with the values located in the same columns as is necessary to run DAD's version of MOSFIT.

Columns 1 to 15—ID

Columns 21 to 30—VGG

Columns 31 to 40—VDD

Columns 41 to 50—VSS

Columns 51 to 60—VBB

Columns 60+—do not care.

Comments may be added to the file by inserting '**' in the first two columns of the line.

The measured data should contain at least three different VBB biases to obtain the best fit. Although a better fit results from more data points, it must be remembered that 2000 points is the maximum number allowable.

IX. PARAMETER INPUT FILE

The included file FITPAR is an example of an acceptable parameter file. Note that in this file:

1. Comments may be included using '**' in the first two columns
2. Input fields are delimited by '||'
3. Some instructions are included in the file
4. Parameter names and order are significant (do not change unless modifying user function MOSEQ)
5. Initial, upper, and lower values are read using an E18.8 format.

If the user wishes to utilize N instead of PHI, he must change the name in the label field from 'PHI' to 'N.'

Any parameter may be fixed by setting the initial, lower and upper bounds to the same value. PHI is commonly set to a fixed value.

X. CONTROL INPUT FILE

The include file FITCON is an example of an acceptable control file. Note that in this file:

1. Comments may be included using '**' in the first two columns
2. Input fields are delimited by '||'
3. Some instructions or comments are included in the file
4. Control variable order is significant (do not change)
5. Values are read using either an I8 or E18.8 format.

The control variables are:

(Suggested)	Name	Explanation
(1.0E-6)	RELTOL	Used in determining requested accuracy
(1.0E-12)	ABSTOL	of fit results
(100)	ITMAX	Maximum number of iterations allowed
(1.0E-6)	IMIN	Smallest measured data, data smaller than this value ignored
(1)	IUNIT	L.U. of output device (1 is terminal, 6 is printer)
(0)	IPRNT	Set to 1 if diagnostics are to be sent to IUNIT, usually set to 0
(1)	METHOD	Fit error reported in percent if 1, fit error reported in AMPS if 0
(2)	INITIAL	Set to 2 if program is to calculate initial values of the parameters, 0 if user's values are to be used
(0)	PMOS	If set to 1, then measured data is negated to become a psuedo-N-channel device
(25)	TEMP	Used in calculating PHI from N

XI. LISTINGS

A. Listing of LODFIT, Transfer File to Set Up FITER.

```
:SV,4,,IH
:AN,
:AN,
:AN,
:AN,
:AN,
:AN, It is assumed that the source file &MOFIT is in the system
:AN, What is the cartridge LU that it resides on? (enter ':,LU')
:PA,1
:SE,,1G
```

```
:AN,
:AN, What LU would you like the relocatable code sent to? (enter ':,LU')
:PA,1
:SE,,,1G
:AN,
:AN, What LU would you like the program to be SP'd on? (enter ':,LU')
:PA,1
:SE,,,,1G
:OF,FITER
:OF,FIN
:OF,PAFIT
:OF,FOUT
:RU,FTN4X,&MOFIT::2G,0,%MOFIT::3G
:RU,LOADR,,%MOFIT::3G
:PU,FIN::4G
:SP,FIN:,4G
:OF,FIN
:PU,FITER::4G
:SP,FITER:,4G
:OF,FITER
:PU,FOUT::4G
:SP,FOUT::4G
:OF,FOUT
:PU,PAFIT::4G
:SP,PAFIT::4G
:OF,PAFIT
:AN,
:AN,        FINISHED SETTING UP FITER ON 4G
:SV,0,,IH
```

B. Listing of FITPAR, FITER Parameter File

```
**                    INPUT PARAMETERS FILE
**    NAME        INITIAL        LOWER        UPPER
      BETA    || 0.40E-4  ||  0.4E-6  ||  0.8E-2  ||
      VTO     || 0.99     ||  00.0    ||  5.0     ||
      PHI     || 0.3600   ||  0.3600  ||  0.3600  ||
      BE      || 0.9      ||  1.0E-6  ||  1.:     ||
      ALPHA   || 1.0      ||  0.1     ||  1.50    ||
      THETA   || 0.1      ||  -1.0    ||  1.50    ||
      LAMDA   || 0.035    ||  -1.0    ||  1.50    ||
      GAMMA   || 0.014    ||  -0.5    ||  1.50    ||
      DE      || 0.04     ||  -0.5    ||  1.50    ||
**        NOTE: IF N IS TO BE USED IN PLACE OF PHI, CHANGE LINE 6 FROM
**              'PHI' TO 'N', LEFT JUSTIFIED.
```

C. Listing of FITCON, FITER Control File

** CONTROL PARAMETERS FILE

** NAME	VALUE			
RELTOL	1.0E−6			
ABSTOL	1.0E−12			
ITMAX	100			
IMIN	1.0E−6			
IUNIT	1	(1=YOUR TERMINAL)	(6=PRINTER(SPOOL))	
IPRNT	0	(1=ERROR STEP)	(0=NO RUN MSGS)	
METHOD	1	(1=RELATIVE ERR)	(2=ABSOLUTE ERROR)	
INITIAL	2	(2=PROGRAM GUESS)	(0=NO INITIAL GUESS)	
PMOS	0	(0=N CHANNEL)	(1=P CHANNEL)	
TEMP	25	(TEMPERATURE IN C)		

D. Example of ASCII Input Data File

EXAMPLE

DATA	VGS	VDS		VBS
0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.2000E+00	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.4000E+00	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.6000E+00	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.8000E+00	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.1000E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.1200E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.1400E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.1600E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.1800E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.2000E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.2200E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.2390E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.2590E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.2790E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.2990E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.3190E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.3390E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.3590E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.3790E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.3990E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.4190E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.4380E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.4580E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.4780E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.4980E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.1000E+01	0.0000E+00	0.0000E+00	0.0000E+00
0.2274E−04	0.1000E+01	0.2000E+00	0.0000E+00	0.0000E+00
0.3534E−04	0.1000E+01	0.4000E+00	0.0000E+00	0.0000E+00
0.3847E−04	0.1000E+01	0.6000E+00	0.0000E+00	0.0000E+00

EXAMPLE

DATA	VGS	VDS		VBS
0.3988E−04	0.1000E+01	0.8000E+00	0.0000E+00	0.0000E+00
0.4123E−04	0.1000E+01	0.1000E+01	0.0000E+00	0.0000E+00
0.4253E−04	0.1000E+01	0.1200E+01	0.0000E+00	0.0000E+00
0.4381E−04	0.1000E+01	0.1400E+01	0.0000E+00	0.0000E+00
0.4506E−04	0.1000E+01	0.1600E+01	0.0000E+00	0.0000E+00
0.4630E−04	0.1000E+01	0.1800E+01	0.0000E+00	0.0000E+00
0.4752E−04	0.1000E+01	0.2000E+01	0.0000E+00	0.0000E+00
0.4874E−04	0.1000E+01	0.2200E+01	0.0000E+00	0.0000E+00
0.4989E−04	0.1000E+01	0.2390E+01	0.0000E+00	0.0000E+00
0.5110E−04	0.1000E+01	0.2590E+01	0.0000E+00	0.0000E+00
0.5230E−04	0.1000E+01	0.2790E+01	0.0000E+00	0.0000E+00
0.5350E−04	0.1000E+01	0.2990E+01	0.0000E+00	0.0000E+00
0.5469E−04	0.1000E+01	0.3190E+01	0.0000E+00	0.0000E+00
0.5589E−04	0.1000E+01	0.3390E+01	0.0000E+00	0.0000E+00
0.5708E−04	0.1000E+01	0.3590E+01	0.0000E+00	0.0000E+00
0.5828E−04	0.1000E+01	0.3790E+01	0.0000E+00	0.0000E+00
0.5948E−04	0.1000E+01	0.3990E+01	0.0000E+00	0.0000E+00
0.6068E−04	0.1000E+01	0.4190E+01	0.0000E+00	0.0000E+00
0.6182E−04	0.1000E+01	0.4380E+01	0.0000E+00	0.0000E+00
0.6302E−04	0.1000E+01	0.4580E+01	0.0000E+00	0.0000E+00
0.6422E−04	0.1000E+01	0.4780E+01	0.0000E+00	0.0000E+00
0.6543E−04	0.1000E+01	0.4980E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.2000E+01	0.0000E+00	0.0000E+00	0.0000E+00
0.7100E−04	0.2000E+01	0.2000E+00	0.0000E+00	0.0000E+00
0.1321E−03	0.2000E+01	0.4000E+00	0.0000E+00	0.0000E+00
0.1831E−03	0.2000E+01	0.6000E+00	0.0000E+00	0.0000E+00
0.2238E−03	0.2000E+01	0.8000E+00	0.0000E+00	0.0000E+00
0.2543E−03	0.2000E+01	0.1000E+01	0.0000E+00	0.0000E+00
0.2745E−03	0.2000E+01	0.1200E+01	0.0000E+00	0.0000E+00
0.2843E−03	0.2000E+01	0.1400E+01	0.0000E+00	0.0000E+00
0.2886E−03	0.2000E+01	0.1600E+01	0.0000E+00	0.0000E+00
0.2936E−03	0.2000E+01	0.1800E+01	0.0000E+00	0.0000E+00
0.2985E−03	0.2000E+01	0.2000E+01	0.0000E+00	0.0000E+00
0.3034E−03	0.2000E+01	0.2200E+01	0.0000E+00	0.0000E+00
0.3080E−03	0.2000E+01	0.2390E+01	0.0000E+00	0.0000E+00
0.3129E−03	0.2000E+01	0.2590E+01	0.0000E+00	0.0000E+00
0.3178E−03	0.2000E+01	0.2790E+01	0.0000E+00	0.0000E+00
0.3226E−03	0.2000E+01	0.2990E+01	0.0000E+00	0.0000E+00
0.3274E−03	0.2000E+01	0.3190E+01	0.0000E+00	0.0000E+00
0.3323E−03	0.2000E+01	0.3390E+01	0.0000E+00	0.0000E+00
0.3371E−03	0.2000E+01	0.3590E+01	0.0000E+00	0.0000E+00
0.3419E−03	0.2000E+01	0.3790E+01	0.0000E+00	0.0000E+00
0.3467E−03	0.2000E+01	0.3990E+01	0.0000E+00	0.0000E+00
0.3515E−03	0.2000E+01	0.4190E+01	0.0000E+00	0.0000E+00
0.3561E−03	0.2000E+01	0.4380E+01	0.0000E+00	0.0000E+00
0.3609E−03	0.2000E+01	0.4580E+01	0.0000E+00	0.0000E+00
0.3657E−03	0.2000E+01	0.4780E+01	0.0000E+00	0.0000E+00
0.3705E−03	0.2000E+01	0.4980E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.3000E+01	0.0000E+00	0.0000E+00	0.0000E+00
0.1105E−03	0.3000E+01	0.2000E+00	0.0000E+00	0.0000E+00
0.2111E−03	0.3000E+01	0.4000E+00	0.0000E+00	0.0000E+00
0.3017E−03	0.3000E+01	0.6000E+00	0.0000E+00	0.0000E+00
0.3821E−03	0.3000E+01	0.8000E+00	0.0000E+00	0.0000E+00
0.4524E−03	0.3000E+01	0.1000E+01	0.0000E+00	0.0000E+00

EXAMPLE

DATA	VGS	VDS		VBS
0.5125E−03	0.3000E+01	0.1200E+01	0.0000E+00	0.0000E+00
0.5624E−03	0.3000E+01	0.1400E+01	0.0000E+00	0.0000E+00
0.6020E−03	0.3000E+01	0.1600E+01	0.0000E+00	0.0000E+00
0.6313E−03	0.3000E+01	0.1800E+01	0.0000E+00	0.0000E+00
0.6504E−03	0.3000E+01	0.2000E+01	0.0000E+00	0.0000E+00
0.6593E−03	0.3000E+01	0.2200E+01	0.0000E+00	0.0000E+00
0.6660E−03	0.3000E+01	0.2390E+01	0.0000E+00	0.0000E+00
0.6747E−03	0.3000E+01	0.2590E+01	0.0000E+00	0.0000E+00
0.6834E−03	0.3000E+01	0.2790E+01	0.0000E+00	0.0000E+00
0.6920E−03	0.3000E+01	0.2990E+01	0.0000E+00	0.0000E+00
0.7007E−03	0.3000E+01	0.3190E+01	0.0000E+00	0.0000E+00
0.7093E−03	0.3000E+01	0.3390E+01	0.0000E+00	0.0000E+00
0.7179E−03	0.3000E+01	0.3590E+01	0.0000E+00	0.0000E+00
0.7265E−03	0.3000E+01	0.3790E+01	0.0000E+00	0.0000E+00
0.7351E−03	0.3000E+01	0.3990E+01	0.0000E+00	0.0000E+00
0.7437E−03	0.3000E+01	0.4190E+01	0.0000E+00	0.0000E+00
0.7518E−03	0.3000E+01	0.4380E+01	0.0000E+00	0.0000E+00
0.7604E−03	0.3000E+01	0.4580E+01	0.0000E+00	0.0000E+00
0.7690E−03	0.3000E+01	0.4780E+01	0.0000E+00	0.0000E+00
0.7775E−03	0.3000E+01	0.4980E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.4000E+01	0.0000E+00	0.0000E+00	0.0000E+00
0.1450E−03	0.4000E+01	0.2000E+00	0.0000E+00	0.0000E+00
0.2801E−03	0.4000E+01	0.4000E+00	0.0000E+00	0.0000E+00
0.4050E−03	0.4000E+01	0.6000E+00	0.0000E+00	0.0000E+00
0.5198E−03	0.4000E+01	0.8000E+00	0.0000E+00	0.0000E+00
0.6244E−03	0.4000E+01	0.1000E+01	0.0000E+00	0.0000E+00
0.7188E−03	0.4000E+01	0.1200E+01	0.0000E+00	0.0000E+00
0.8028E−03	0.4000E+01	0.1400E+01	0.0000E+00	0.0000E+00
0.8766E−03	0.4000E+01	0.1600E+01	0.0000E+00	0.0000E+00
0.9401E−03	0.4000E+01	0.1800E+01	0.0000E+00	0.0000E+00
0.9933E−03	0.4000E+01	0.2000E+01	0.0000E+00	0.0000E+00
0.1036E−02	0.4000E+01	0.2200E+01	0.0000E+00	0.0000E+00
0.1067E−02	0.4000E+01	0.2390E+01	0.0000E+00	0.0000E+00
0.1090E−02	0.4000E+01	0.2590E+01	0.0000E+00	0.0000E+00
0.1103E−02	0.4000E+01	0.2790E+01	0.0000E+00	0.0000E+00
0.1110E−02	0.4000E+01	0.2990E+01	0.0000E+00	0.0000E+00
0.1122E−02	0.4000E+01	0.3190E+01	0.0000E+00	0.0000E+00
0.1134E−02	0.4000E+01	0.3390E+01	0.0000E+00	0.0000E+00
0.1146E−02	0.4000E+01	0.3590E+01	0.0000E+00	0.0000E+00
0.1158E−02	0.4000E+01	0.3790E+01	0.0000E+00	0.0000E+00
0.1170E−02	0.4000E+01	0.3990E+01	0.0000E+00	0.0000E+00
0.1181E−02	0.4000E+01	0.4190E+01	0.0000E+00	0.0000E+00
0.1193E−02	0.4000E+01	0.4380E+01	0.0000E+00	0.0000E+00
0.1205E−02	0.4000E+01	0.4580E+01	0.0000E+00	0.0000E+00
0.1216E−02	0.4000E+01	0.4780E+01	0.0000E+00	0.0000E+00
0.1228E−02	0.4000E+01	0.4980E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.5000E+01	0.0000E+00	0.0000E+00	0.0000E+00
0.1764E−03	0.5000E+01	0.2000E+00	0.0000E+00	0.0000E+00
0.3428E−03	0.5000E+01	0.4000E+00	0.0000E+00	0.0000E+00
0.4989E−03	0.5000E+01	0.6000E+00	0.0000E+00	0.0000E+00
0.6447E−03	0.5000E+01	0.8000E+00	0.0000E+00	0.0000E+00
0.7802E−03	0.5000E+01	0.1000E+01	0.0000E+00	0.0000E+00
0.9052E−03	0.5000E+01	0.1200E+01	0.0000E+00	0.0000E+00
0.1020E−02	0.5000E+01	0.1400E+01	0.0000E+00	0.0000E+00

EXAMPLE

DATA	VGS	VDS		VBS
0.1124E−02	0.5000E+01	0.1600E+01	0.0000E+00	0.0000E+00
0.1218E−02	0.5000E+01	0.1800E+01	0.0000E+00	0.0000E+00
0.1301E−02	0.5000E+01	0.2000E+01	0.0000E+00	0.0000E+00
0.1374E−02	0.5000E+01	0.2200E+01	0.0000E+00	0.0000E+00
0.1434E−02	0.5000E+01	0.2390E+01	0.0000E+00	0.0000E+00
0.1487E−02	0.5000E+01	0.2590E+01	0.0000E+00	0.0000E+00
0.1529E−02	0.5000E+01	0.2790E+01	0.0000E+00	0.0000E+00
0.1561E−02	0.5000E+01	0.2990E+01	0.0000E+00	0.0000E+00
0.1582E−02	0.5000E+01	0.3190E+01	0.0000E+00	0.0000E+00
0.1592E−02	0.5000E+01	0.3390E+01	0.0000E+00	0.0000E+00
0.1602E−02	0.5000E+01	0.3590E+01	0.0000E+00	0.0000E+00
0.1617E−02	0.5000E+01	0.3790E+01	0.0000E+00	0.0000E+00
0.1632E−02	0.5000E+01	0.3990E+01	0.0000E+00	0.0000E+00
0.1646E−02	0.5000E+01	0.4190E+01	0.0000E+00	0.0000E+00
0.1660E−02	0.5000E+01	0.4380E+01	0.0000E+00	0.0000E+00
0.1675E−02	0.5000E+01	0.4580E+01	0.0000E+00	0.0000F+00
0.1689E−02	0.5000E+01	0.4780E+01	0.0000E+00	0.0000E+00
0.1704E−02	0.5000E+01	0.4980E+01	0.0000E+00	0.0000E+00
0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.2000E+00	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.4000E+00	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.6000E+00	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.8000E+00	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.1000E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.1200E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.1400E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.1600E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.1800E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.2000E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.2200E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.2390E+01	0.0000E+00	−0.1000F+01
0.0000E+00	0.0000E+00	0.2590E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.2790E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.2990E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.3190E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.3390E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.3590E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.3790E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.3990E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.4190E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.4380E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.4580E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.4780E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.4980E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.1000E+01	0.0000E+00	0.0000E+00	−0.1000E+01
0.1984E−04	0.1000E+01	0.2000E+00	0.0000E+00	−0.1000E+01
0.2951E−04	0.1000E+01	0.4000E+00	0.0000E+00	−0.1000E+01
0.3128E−04	0.1000E+01	0.6000E+00	0.0000E+00	−0.1000E+01
0.3252E−04	0.1000E+01	0.8000E+00	0.0000E+00	−0.1000E+01
0.3369E−04	0.1000E+01	0.1000E+01	0.0000E+00	−0.1000E+01
0.3483E−04	0.1000E+01	0.1200E+01	0.0000E+00	−0.1000E+01
0.3594E−04	0.1000E+01	0.1400E+01	0.0000E+00	−0.1000E+01
0.3703E−04	0.1000E+01	0.1600E+01	0.0000E+00	−0.1000E+01
0.3811E−04	0.1000E+01	0.1800E+01	0.0000E+00	−0.1000E+01

EXAMPLE

DATA	VGS	VDS		VBS
0.3917E−04	0.1000E+01	0.2000E+01	0.0000E+00	−0.1000E+01
0.4023E−04	0.1000E+01	0.2200E+01	0.0000E+00	−0.1000E+01
0.4123E−04	0.1000E+01	0.2390E+01	0.0000E+00	−0.1000E+01
0.4228E−04	0.1000E+01	0.2590E+01	0.0000E+00	−0.1000E+01
0.4332E−04	0.1000E+01	0.2790E+01	0.0000E+00	−0.1000E+01
0.4436E−04	0.1000E+01	0.2990E+01	0.0000E+00	−0.1000E+01
0.4540E−04	0.1000E+01	0.3190E+01	0.0000E+00	−0.1000E+01
0.4645E−04	0.1000E+01	0.3390E+01	0.0000E+00	−0.1000E+01
0.4749E−04	0.1000E+01	0.3590E+01	0.0000E+00	−0.1000E+01
0.4853E−04	0.1000E+01	0.3790E+01	0.0000E+00	−0.1000E+01
0.4957E−04	0.1000E+01	0.3990E+01	0.0000E+00	−0.1000E+01
0.5062E−04	0.1000E+01	0.4190E+01	0.0000E+00	−0.1000E+01
0.5161E−04	0.1000E+01	0.4380E+01	0.0000E+00	−0.1000E+01
0.5266E−04	0.1000E+01	0.4580E+01	0.0000E+00	−0.1000E+01
0.5371E−04	0.1000E+01	0.4780E+01	0.0000E+00	−0.1000E+01
0.5476E−04	0.1000E+01	0.4980E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.2000E+01	0.0000E+00	0.0000E+00	−0.1000E+01
0.6873E−04	0.2000E+01	0.2000E+00	0.0000E+00	−0.1000E+01
0.1276E−03	0.2000E+01	0.4000E+00	0.0000E+00	−0.1000E+01
0.1763E−03	0.2000E+01	0.6000E+00	0.0000E+00	−0.1000E+01
0.2147E−03	0.2000E+01	0.8000E+00	0.0000E+00	−0.1000E+01
0.2429E−03	0.2000E+01	0.1000E+01	0.0000E+00	−0.1000E+01
0.2607E−03	0.2000E+01	0.1200E+01	0.0000E+00	−0.1000E+01
0.2683E−03	0.2000E+01	0.1400E+01	0.0000E+00	−0.1000E+01
0.2727E−03	0.2000E+01	0.1600E+01	0.0000E+00	−0.1000E+01
0.2775E−03	0.2000E+01	0.1800E+01	0.0000E+00	−0.1000E+01
0.2822E−03	0.2000E+01	0.2000E+01	0.0000E+00	−0.1000E+01
0.2869E−03	0.2000E+01	0.2200E+01	0.0000E+00	−0.1000E+01
0.2913E−03	0.2000E+01	0.2390E+01	0.0000E+00	−0.1000E+01
0.2960E−03	0.2000E+01	0.2590E+01	0.0000E+00	−0.1000E+01
0.3006E−03	0.2000E+01	0.2790E+01	0.0000E+00	−0.1000E+01
0.3053E−03	0.2000E+01	0.2990E+01	0.0000E+00	−0.1000E+01
0.3099E−03	0.2000E+01	0.3190E+01	0.0000E+00	−0.1000E+01
0.3145E−03	0.2000E+01	0.3390E+01	0.0000E+00	−0.1000E+01
0.3191E−03	0.2000E+01	0.3590E+01	0.0000E+00	−0.1000E+01
0.3238E−03	0.2000E+01	0.3790E+01	0.0000E+00	−0.1000E+01
0.3284E−03	0.2000E+01	0.3990E+01	0.0000E+00	−0.1000E+01
0.3330E−03	0.2000E+01	0.4190E+01	0.0000E+00	−0.1000E+01
0.3373E−03	0.2000E+01	0.4380E+01	0.0000E+00	−0.1000E+01
0.3419E−03	0.2000E+01	0.4580E+01	0.0000E+00	−0.1000E+01
0.3465E−03	0.2000E+01	0.4780E+01	0.0000E+00	−0.1000E+01
0.3511E−03	0.2000E+01	0.4980E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.3000E+01	0.0000E+00	0.0000E+00	−0.1000E+01
0.1086E−03	0.3000E+01	0.2000E+00	0.0000E+00	−0.1000E+01
0.2073E−03	0.3000E+01	0.4000E+00	0.0000E+00	−0.1000E+01
0.2959E−03	0.3000E+01	0.6000E+00	0.0000E+00	−0.1000E+01
0.3744E−03	0.3000E+01	0.8000E+00	0.0000E+00	−0.1000E+01
0.4428E−03	0.3000E+01	0.1000E+01	0.0000E+00	−0.1000E+01
0.5009E−03	0.3000E+01	0.1200E+01	0.0000E+00	−0.1000E+01
0.5489E−03	0.3000E+01	0.1400E+01	0.0000E+00	−0.1000E+01
0.5866E−03	0.3000E+01	0.1600E+01	0.0000E+00	−0.1000E+01
0.6140E−03	0.3000E+01	0.1800E+01	0.0000E+00	−0.1000E+01
0.6312E−03	0.3000E+01	0.2000E+01	0.0000E+00	−0.1000E+01
0.6380E−03	0.3000E+01	0.2200E+01	0.0000E+00	−0.1000E+01

EXAMPLE

DATA	VGS	VDS		VBS
0.6458E−03	0.3000E+01	0.2390E+01	0.0000E+00	−0.1000E+01
0.6543E−03	0.3000E+01	0.2590E+01	0.0000E+00	−0.1000E+01
0.6628E−03	0.3000E+01	0.2790E+01	0.0000E+00	−0.1000E+01
0.6712E−03	0.3000E+01	0.2990E+01	0.0000E+00	−0.1000E+01
0.6797E−03	0.3000E+01	0.3190E+01	0.0000E+00	−0.1000E+01
0.6881E−03	0.3000E+01	0.3390E+01	0.0000E+00	−0.1000E+01
0.6965E−03	0.3000E+01	0.3590E+01	0.0000E+00	−0.1000E+01
0.7049E−03	0.3000E+01	0.3790E+01	0.0000E+00	−0.1000E+01
0.7133E−03	0.3000E+01	0.3990E+01	0.0000E+00	−0.1000E+01
0.7217E−03	0.3000E+01	0.4190E+01	0.0000E+00	−0.1000E+01
0.7297E−03	0.3000E+01	0.4380E+01	0.0000E+00	−0.1000E+01
0.7381E−03	0.3000E+01	0.4580E+01	0.0000E+00	−0.1000E+01
0.7464E−03	0.3000E+01	0.4780E+01	0.0000E+00	−0.1000E+01
0.7548E−03	0.3000E+01	0.4980E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.4000E+01	0.0000E+00	0.0000E+00	−0.1000E+01
0.1433E−03	0.4000E+01	0.2000E+00	0.0000E+00	−0.1000E+01
0.2766E−03	0.4000E+01	0.4000E+00	0.0000E+00	−0.1000E+01
0.3999E−03	0.4000E+01	0.6000E+00	0.0000E+00	−0.1000E+01
0.5130E−03	0.4000E+01	0.8000E+00	0.0000E+00	−0.1000E+01
0.6159E−03	0.4000E+01	0.1000E+01	0.0000E+00	−0.1000E+01
0.7085E−03	0.4000E+01	0.1200E+01	0.0000E+00	−0.1000E+01
0.7909E−03	0.4000E+01	0.1400E+01	0.0000E+00	−0.1000E+01
0.8630E−03	0.4000E+01	0.1600E+01	0.0000E+00	−0.1000E+01
0.9248E−03	0.4000E+01	0.1800E+01	0.0000E+00	−0.1000E+01
0.9763E−03	0.4000E+01	0.2000E+01	0.0000E+00	−0.1000E+01
0.1018E−02	0.4000E+01	0.2200E+01	0.0000E+00	−0.1000E+01
0.1047E−02	0.4000E+01	0.2390E+01	0.0000E+00	−0.1000E+01
0.1068E−02	0.4000E+01	0.2590E+01	0.0000E+00	−0.1000E+01
0.1079E−02	0.4000E+01	0.2790E+01	0.0000E+00	−0.1000E+01
0.1087E−02	0.4000E+01	0.2990E+01	0.0000E+00	−0.1000E+01
0.1099E−02	0.4000E+01	0.3190E+01	0.0000E+00	−0.1000E+01
0.1111E−02	0.4000E+01	0.3390E+01	0.0000E+00	−0.1000E+01
0.1123E−02	0.4000E+01	0.3590E+01	0.0000E+00	−0.1000E+01
0.1134E−02	0.4000E+01	0.3790E+01	0.0000E+00	−0.1000E+01
0.1146E−02	0.4000E+01	0.3990E+01	0.0000E+00	−0.1000E+01
0.1158E−02	0.4000E+01	0.4190E+01	0.0000E+00	−0.1000E+01
0.1169E−02	0.4000E+01	0.4380E+01	0.0000E+00	−0.1000E+01
0.1181E−02	0.4000E+01	0.4580E+01	0.0000E+00	−0.1000E+01
0.1192E−02	0.4000E+01	0.4780E+01	0.0000E+00	−0.1000E+01
0.1204E−02	0.4000E+01	0.4980E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.5000E+01	0.0000E+00	0.0000E+00	−0.1000E+01
0.1748E−03	0.5000E+01	0.2000E+00	0.0000E+00	−0.1000E+01
0.3396E−03	0.5000E+01	0.4000E+00	0.0000E+00	−0.1000E+01
0.4942E−03	0.5000E+01	0.6000E+00	0.0000E+00	−0.1000E+01
0.6384E−03	0.5000E+01	0.8000E+00	0.0000E+00	−0.1000E+01
0.7723E−03	0.5000E+01	0.1000E+01	0.0000E+00	−0.1000E+01
0.8958E−03	0.5000E+01	0.1200E+01	0.0000E+00	−0.1000E+01
0.1009E−02	0.5000E+01	0.1400E+01	0.0000E+00	−0.1000E+01
0.1112E−02	0.5000E+01	0.1600E+01	0.0000E+00	−0.1000E+01
0.1204E−02	0.5000E+01	0.1800E+01	0.0000E+00	−0.1000E+01
0.1286E−02	0.5000E+01	0.2000E+01	0.0000E+00	−0.1000E+01
0.1357E−02	0.5000E+01	0.2200E+01	0.0000E+00	−0.1000E+01
0.1416E−02	0.5000E+01	0.2390E+01	0.0000E+00	−0.1000E+01
0.1467E−02	0.5000E+01	0.2590E+01	0.0000E+00	−0.1000E+01

EXAMPLE

DATA	VGS	VDS		VBS
0.1507E−02	0.5000E+01	0.2790E+01	0.0000E+00	−0.1000E+01
0.1538E−02	0.5000E+01	0.2990E+01	0.0000E+00	−0.1000E+01
0.1557E−02	0.5000E+01	0.3190E+01	0.0000E+00	−0.1000E+01
0.1567E−02	0.5000E+01	0.3390E+01	0.0000E+00	−0.1000E+01
0.1578E−02	0.5000E+01	0.3590E+01	0.0000E+00	−0.1000E+01
0.1592E−02	0.5000E+01	0.3790E+01	0.0000E+00	−0.1000E+01
0.1607E−02	0.5000E+01	0.3990E+01	0.0000E+00	−0.1000E+01
0.1621E−02	0.5000E+01	0.4190E+01	0.0000E+00	−0.1000E+01
0.1635E−02	0.5000E+01	0.4380E+01	0.0000E+00	−0.1000E+01
0.1649E−02	0.5000E+01	0.4580E+01	0.0000E+00	−0.1000E+01
0.1664E−02	0.5000E+01	0.4780E+01	0.0000E+00	−0.1000E+01
0.1678E−02	0.5000E+01	0.4980E+01	0.0000E+00	−0.1000E+01
0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.2000E+00	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.4000E+00	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.6000E+00	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.8000E+00	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.1000E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.1200E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.1400E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.1600E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.1800E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.2000E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.2200E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.2390E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.2590E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.2790E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.2990E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.3190E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.3390E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.3590E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.3790E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.3990E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.4190E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.4380E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.4580E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.4780E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.4980E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.1000E+01	0.0000E+00	0.0000E+00	−0.2000E+01
0.1769E−04	0.1000E+01	0.2000E+00	0.0000E+00	−0.2000E+01
0.2520E−04	0.1000E+01	0.4000E+00	0.0000E+00	−0.2000E+01
0.2644E−04	0.1000E+01	0.6000E+00	0.0000E+00	−0.2000E+01
0.2755E−04	0.1000E+01	0.8000E+00	0.0000E+00	−0.2000E+01
0.2860E−04	0.1000E+01	0.1000E+01	0.0000E+00	−0.2000E+01
0.2962E−04	0.1000E+01	0.1200E+01	0.0000E+00	−0.2000E+01
0.3061E−04	0.1000E+01	0.1400E+01	0.0000E+00	−0.2000E+01
0.3159E−04	0.1000E+01	0.1600E+01	0.0000E+00	−0.2000E+01
0.3255E−04	0.1000E+01	0.1800E+01	0.0000E+00	−0.2000E+01
0.3350E−04	0.1000E+01	0.2000E+01	0.0000E+00	−0.2000E+01
0.3445E−04	0.1000E+01	0.2200E+01	0.0000E+00	−0.2000E+01
0.3534E−04	0.1000E+01	0.2390E+01	0.0000E+00	−0.2000E+01
0.3628E−04	0.1000E+01	0.2590E+01	0.0000E+00	−0.2000E+01
0.3721E−04	0.1000E+01	0.2790E+01	0.0000E+00	−0.2000E+01
0.3815E−04	0.1000E+01	0.2990E+01	0.0000E+00	−0.2000E+01

EXAMPLE

DATA	VGS	VDS		VBS
0.3908E−04	0.1000E+01	0.3190E+01	0.0000E+00	−0.2000E+01
0.4001E−04	0.1000E+01	0.3390E+01	0.0000E+00	−0.2000E+01
0.4094E−04	0.1000E+01	0.3590E+01	0.0000E+00	−0.2000E+01
0.4188E−04	0.1000E+01	0.3790E+01	0.0000E+00	−0.2000E+01
0.4281E−04	0.1000E+01	0.3990E+01	0.0000E+00	−0.2000E+01
0.4374E−04	0.1000E+01	0.4190E+01	0.0000E+00	−0.2000E+01
0.4464E−04	0.1000E+01	0.4380E+01	0.0000E+00	−0.2000E+01
0.4557E−04	0.1000E+01	0.4580E+01	0.0000E+00	−0.2000E+01
0.4652E−04	0.1000E+01	0.4780E+01	0.0000E+00	−0.2000E+01
0.4746E−04	0.1000E+01	0.4980E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.2000E+01	0.0000E+00	0.0000E+00	−0.2000E+01
0.6707E−04	0.2000E+01	0.2000E+00	0.0000E+00	−0.2000E+01
0.1242E−03	0.2000E+01	0.4000E+00	0.0000E+00	−0.2000E+01
0.1712E−03	0.2000E+01	0.6000E+00	0.0000E+00	−0.2000E+01
0.2080E−03	0.2000E+01	0.8000E+00	0.0000E+00	−0.2000E+01
0.2345E−03	0.2000E+01	0.1000E+01	0.0000E+00	−0.2000E+01
0.2506E−03	0.2000E+01	0.1200E+01	0.0000E+00	−0.2000E+01
0.2566E−03	0.2000E+01	0.1400E+01	0.0000E+00	−0.2000E+01
0.2613E−03	0.2000E+01	0.1600E+01	0.0000E+00	−0.2000E+01
0.2659E−03	0.2000E+01	0.1800E+01	0.0000E+00	−0.2000E+01
0.2704E−03	0.2000E+01	0.2000E+01	0.0000E+00	−0.2000E+01
0.2750E−03	0.2000E+01	0.2200E+01	0.0000E+00	−0.2000E+01
0.2793E−03	0.2000E+01	0.2390E+01	0.0000E+00	−0.2000E+01
0.2838E−03	0.2000E+01	0.2590E+01	0.0000E+00	−0.2000E+01
0.2883E−03	0.2000E+01	0.2790E+01	0.0000E+00	−0.2000E+01
0.2928E−03	0.2000E+01	0.2990E+01	0.0000E+00	−0.2000E+01
0.2973E−03	0.2000E+01	0.3190E+01	0.0000E+00	−0.2000E+01
0.3017E−03	0.2000E+01	0.3390E+01	0.0000E+00	−0.2000E+01
0.3062E−03	0.2000E+01	0.3590E+01	0.0000E+00	−0.2000E+01
0.3107E−03	0.2000E+01	0.3790E+01	0.0000E+00	−0.2000E+01
0.3151E−03	0.2000E+01	0.3990E+01	0.0000E+00	−0.2000E+01
0.3196E−03	0.2000E+01	0.4190E+01	0.0000E+00	−0.2000E+01
0.3238E−03	0.2000E+01	0.4380E+01	0.0000E+00	−0.2000E+01
0.3283E−03	0.2000E+01	0.4580E+01	0.0000E+00	−0.2000E+01
0.3327E−03	0.2000E+01	0.4780E+01	0.0000E+00	−0.2000E+01
0.3372E−03	0.2000E+01	0.4980E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.3000E+01	0.0000E+00	0.0000E+00	−0.2000E+01
0.1071E−03	0.3000E+01	0.2000E+00	0.0000E+00	−0.2000E+01
0.2044E−03	0.3000E+01	0.4000E+00	0.0000E+00	−0.2000E+01
0.2917E−03	0.3000E+01	0.6000E+00	0.0000E+00	−0.2000E+01
0.3688E−03	0.3000E+01	0.8000E+00	0.0000E+00	−0.2000E+01
0.4357E−03	0.3000E+01	0.1000E+01	0.0000E+00	−0.2000E+01
0.4925E−03	0.3000E+01	0.1200E+01	0.0000E+00	−0.2000E+01
0.5390E−03	0.3000E+01	0.1400E+01	0.0000E+00	−0.2000E+01
0.5752E−03	0.3000E+01	0.1600E+01	0.0000E+00	−0.2000E+01
0.6013E−03	0.3000E+01	0.1800E+01	0.0000E+00	−0.2000E+01
0.6170E−03	0.3000E+01	0.2000E+01	0.0000E+00	−0.2000E+01
0.6231E−03	0.3000E+01	0.2200E+01	0.0000E+00	−0.2000E+01
0.6311E−03	0.3000E+01	0.2390E+01	0.0000E+00	−0.2000E+01
0.6395E−03	0.3000E+01	0.2590E+01	0.0000E+00	−0.2000E+01
0.6478E−03	0.3000E+01	0.2790E+01	0.0000E+00	−0.2000E+01
0.6561E−03	0.3000E+01	0.2990E+01	0.0000E+00	−0.2000E+01
0.6644E−03	0.3000E+01	0.3190E+01	0.0000E+00	−0.2000E+01
0.6727E−03	0.3000E+01	0.3390E+01	0.0000E+00	−0.2000E+01

EXAMPLE

DATA	VGS	VDS		VBS
0.6810E−03	0.3000E+01	0.3590E+01	0.0000E+00	−0.2000E+01
0.6893E−03	0.3000E+01	0.3790E+01	0.0000E+00	−0.2000E+01
0.6975E−03	0.3000E+01	0.3990E+01	0.0000E+00	−0.2000E+01
0.7058E−03	0.3000E+01	0.4190E+01	0.0000E+00	−0.2000E+01
0.7136E−03	0.3000E+01	0.4380E+01	0.0000E+00	−0.2000E+01
0.7219E−03	0.3000E+01	0.4580E+01	0.0000E+00	−0.2000E+01
0.7301E−03	0.3000E+01	0.4780E+01	0.0000E+00	−0.2000E+01
0.7383E−03	0.3000E+01	0.4980E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.4000E+01	0.0000E+00	0.0000E+00	−0.2000E+01
0.1420E−03	0.4000E+01	0.2000E+00	0.0000E+00	−0.2000E+01
0.2741E−03	0.4000E+01	0.4000E+00	0.0000E+00	−0.2000E+01
0.3961E−03	0.4000E+01	0.6000E+00	0.0000E+00	−0.2000E+01
0.5080E−03	0.4000E+01	0.8000E+00	0.0000E+00	−0.2000E+01
0.6096E−03	0.4000E+01	0.1000E+01	0.0000E+00	−0.2000E+01
0.7010E−03	0.4000E+01	0.1200E+01	0.0000E+00	−0.2000E+01
0.7821E−03	0.4000E+01	0.1400E+01	0.0000E+00	−0.2000E+01
0.8530E−03	0.4000E+01	0.1600E+01	0.0000E+00	−0.2000E+01
0.9136E−03	0.4000E+01	0.1800E+01	0.0000E+00	−0.2000E+01
0.9639E−03	0.4000E+01	0.2000E+01	0.0000E+00	−0.2000E+01
0.1004E−02	0.4000E+01	0.2200E+01	0.0000E+00	−0.2000E+01
0.1032E−02	0.4000E+01	0.2390E+01	0.0000E+00	−0.2000E+01
0.1052E−02	0.4000E+01	0.2590E+01	0.0000E+00	−0.2000E+01
0.1062E−02	0.4000E+01	0.2790E+01	0.0000E+00	−0.2000E+01
0.1071E−02	0.4000E+01	0.2990E+01	0.0000E+00	−0.2000E+01
0.1082E−02	0.4000E+01	0.3190E+01	0.0000E+00	−0.2000E+01
0.1094E−02	0.4000E+01	0.3390E+01	0.0000E+00	−0.2000E+01
0.1106E−02	0.4000E+01	0.3590E+01	0.0000E+00	−0.2000E+01
0.1117E−02	0.4000E+01	0.3790E+01	0.0000E+00	−0.2000E+01
0.1129E−02	0.4000E+01	0.3990E+01	0.0000E+00	−0.2000E+01
0.1141E−02	0.4000E+01	0.4190E+01	0.0000E+00	−0.2000E+01
0.1152E−02	0.4000E+01	0.4380E+01	0.0000E+00	−0.2000E+01
0.1163E−02	0.4000E+01	0.4580E+01	0.0000E+00	−0.2000E+01
0.1175E−02	0.4000E+01	0.4780E+01	0.0000E+00	−0.2000E+01
0.1186E−02	0.4000E+01	0.4980E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.5000E+01	0.0000E+00	0.0000E+00	−0.2000E+01
0.1737E−03	0.5000E+01	0.2000E+00	0.0000E+00	−0.2000E+01
0.3373E−03	0.5000E+01	0.4000E+00	0.0000E+00	−0.2000E+01
0.4907E−03	0.5000E+01	0.6000E+00	0.0000E+00	−0.2000E+01
0.6338E−03	0.5000E+01	0.8000E+00	0.0000E+00	−0.2000E+01
0.7665E−03	0.5000E+01	0.1000E+01	0.0000E+00	−0.2000E+01
0.8889E−03	0.5000E+01	0.1200E+01	0.0000E+00	−0.2000E+01
0.1001E−02	0.5000E+01	0.1400E+01	0.0000E+00	−0.2000E+01
0.1103E−02	0.5000E+01	0.1600E+01	0.0000E+00	−0.2000E+01
0.1194E−02	0.5000E+01	0.1800E+01	0.0000E+00	−0.2000E+01
0.1275E−02	0.5000E+01	0.2000E+01	0.0000E+00	−0.2000E+01
0.1345E−02	0.5000E+01	0.2200E+01	0.0000E+00	−0.2000E+01
0.1402E−02	0.5000E+01	0.2390E+01	0.0000E+00	−0.2000E+01
0.1452E−02	0.5000E+01	0.2590E+01	0.0000E+00	−0.2000E+01
0.1492E−02	0.5000E+01	0.2790E+01	0.0000E+00	−0.2000E+01
0.1521E−02	0.5000E+01	0.2990E+01	0.0000E+00	−0.2000E+01
0.1540E−02	0.5000E+01	0.3190E+01	0.0000E+00	−0.2000E+01
0.1548E−02	0.5000E+01	0.3390E+01	0.0000E+00	−0.2000E+01
0.1560E−02	0.5000E+01	0.3590E+01	0.0000E+00	−0.2000E+01
0.1574E−02	0.5000E+01	0.3790E+01	0.0000E+00	−0.2000E+01

EXAMPLE

DATA	VGS	VDS		VBS
0.1589E−02	0.5000E+01	0.3990E+01	0.0000E+00	−0.2000E+01
0.1603E−02	0.5000E+01	0.4190E+01	0.0000E+00	−0.2000E+01
0.1617E−02	0.5000E+01	0.4380E+01	0.0000E+00	−0.2000E+01
0.1631E−02	0.5000E+01	0.4580E+01	0.0000E+00	−0.2000E+01
0.1645E−02	0.5000E+01	0.4780E+01	0.0000E+00	−0.2000E+01
0.1660E−02	0.5000E+01	0.4980E+01	0.0000E+00	−0.2000E+01
0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.2000E+00	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.4000E+00	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.6000E+00	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.8000E+00	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.1000E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.1200E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.1400E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.1600E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.1800E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.2000E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.2200E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.2390E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.2590E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.2790E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.2990E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.3190E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.3390E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.3590E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.3790E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.3990E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.4190E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.4380E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.4580E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.4780E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.0000E+00	0.4980E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.1000E+01	0.0000E+00	0.0000E+00	−0.3000E+01
0.1589E−04	0.1000E+01	0.2000E+00	0.0000E+00	−0.3000E+01
0.2161E−04	0.1000E+01	0.4000E+00	0.0000E+00	−0.3000E+01
0.2270E−04	0.1000E+01	0.6000E+00	0.0000E+00	−0.3000E+01
0.2370E−04	0.1000E+01	0.8000E+00	0.0000E+00	−0.3000E+01
0.2466E−04	0.1000E+01	0.1000E+01	0.0000E+00	−0.3000E+01
0.2558E−04	0.1000E+01	0.1200E+01	0.0000E+00	−0.3000E+01
0.2648E−04	0.1000E+01	0.1400E+01	0.0000E+00	−0.3000E+01
0.2736E−04	0.1000E+01	0.1600E+01	0.0000E+00	−0.3000E+01
0.2823E−04	0.1000E+01	0.1800E+01	0.0000E+00	−0.3000E+01
0.2909E−04	0.1000E+01	0.2000E+01	0.0000E+00	−0.3000E+01
0.2995E−04	0.1000E+01	0.2200E+01	0.0000E+00	−0.3000E+01
0.3076E−04	0.1000E+01	0.2390E+01	0.0000E+00	−0.3000E+01
0.3161E−04	0.1000E+01	0.2590E+01	0.0000E+00	−0.3000E+01
0.3245E−04	0.1000E+01	0.2790E+01	0.0000E+00	−0.3000E+01
0.3330E−04	0.1000E+01	0.2990E+01	0.0000E+00	−0.3000E+01
0.3414E−04	0.1000E+01	0.3190E+01	0.0000E+00	−0.3000E+01
0.3499E−04	0.1000E+01	0.3390E+01	0.0000E+00	−0.3000E+01
0.3583E−04	0.1000E+01	0.3590E+01	0.0000E+00	−0.3000E+01
0.3668E−04	0.1000E+01	0.3790E+01	0.0000E+00	−0.3000E+01
0.3753E−04	0.1000E+01	0.3990E+01	0.0000E+00	−0.3000E+01
0.3837E−04	0.1000E+01	0.4190E+01	0.0000E+00	−0.3000E+01

EXAMPLE

DATA	VGS	VDS		VBS
0.3918E−04	0.1000E+01	0.4380E+01	0.0000E+00	−0.3000E+01
0.4003E−04	0.1000E+01	0.4580E+01	0.0000E+00	−0.3000E+01
0.4089E−04	0.1000E+01	0.4780E+01	0.0000E+00	−0.3000E+01
0.4175E−04	0.1000E+01	0.4980E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.2000E+01	0.0000E+00	0.0000E+00	−0.3000E+01
0.6568E−04	0.2000E+01	0.2000E+00	0.0000E+00	−0.3000E+01
0.1214E−03	0.2000E+01	0.4000E+00	0.0000E+00	−0.3000E+01
0.1670E−03	0.2000E+01	0.6000E+00	0.0000E+00	−0.3000E+01
0.2024E−03	0.2000E+01	0.8000E+00	0.0000E+00	−0.3000E+01
0.2275E−03	0.2000E+01	0.1000E+01	0.0000E+00	−0.3000E+01
0.2422E−03	0.2000E+01	0.1200E+01	0.0000E+00	−0.3000E+01
0.2474E−03	0.2000E+01	0.1400E+01	0.0000E+00	−0.3000E+01
0.2519E−03	0.2000E+01	0.1600E+01	0.0000E+00	−0.3000E+01
0.2564E−03	0.2000E+01	0.1800E+01	0.0000E+00	−0.3000E+01
0.2608E−03	0.2000E+01	0.2000E+01	0.0000E+00	−0.3000E+01
0.2653E−03	0.2000E+01	0.2200E+01	0.0000E+00	−0.3000E+01
0.2694E−03	0.2000E+01	0.2390E+01	0.0000E+00	−0.3000E+01
0.2738E−03	0.2000E+01	0.2590E+01	0.0000E+00	−0.3000E+01
0.2782E−03	0.2000E+01	0.2790E+01	0.0000E+00	−0.3000E+01
0.2826E−03	0.2000E+01	0.2990E+01	0.0000E+00	−0.3000E+01
0.2869E−03	0.2000E+01	0.3190E+01	0.0000E+00	−0.3000E+01
0.2913E−03	0.2000E+01	0.3390E+01	0.0000E+00	−0.3000E+01
0.2956E−03	0.2000E+01	0.3590E+01	0.0000E+00	−0.3000E+01
0.3000E−03	0.2000E+01	0.3790E+01	0.0000E+00	−0.3000E+01
0.3043E−03	0.2000E+01	0.3990E+01	0.0000E+00	−0.3000E+01
0.3086E−03	0.2000E+01	0.4190E+01	0.0000E+00	−0.3000E+01
0.3128E−03	0.2000E+01	0.4380E+01	0.0000E+00	−0.3000E+01
0.3171E−03	0.2000E+01	0.4580E+01	0.0000E+00	−0.3000E+01
0.3214E−03	0.2000E+01	0.4780E+01	0.0000E+00	−0.3000E+01
0.3257E−03	0.2000E+01	0.4980E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.3000E+01	0.0000E+00	0.0000E+00	−0.3000E+01
0.1060E−03	0.3000E+01	0.2000E+00	0.0000E+00	−0.3000E+01
0.2021E−03	0.3000E+01	0.4000E+00	0.0000E+00	−0.3000E+01
0.2882E−03	0.3000E+01	0.6000E+00	0.0000E+00	−0.3000E+01
0.3641E−03	0.3000E+01	0.8000E+00	0.0000E+00	−0.3000E+01
0.4299E−03	0.3000E+01	0.1000E+01	0.0000E+00	−0.3000E+01
0.4854E−03	0.3000E+01	0.1200E+01	0.0000E+00	−0.3000E+01
0.5307E−03	0.3000E+01	0.1400E+01	0.0000E+00	−0.3000E+01
0.5658E−03	0.3000E+01	0.1600E+01	0.0000E+00	−0.3000E+01
0.5907E−03	0.3000E+01	0.1800E+01	0.0000E+00	−0.3000E+01
0.6052E−03	0.3000E+01	0.2000E+01	0.0000E+00	−0.3000E+01
0.6111E−03	0.3000E+01	0.2200E+01	0.0000E+00	−0.3000E+01
0.6190E−03	0.3000E+01	0.2390E+01	0.0000E+00	−0.3000E+01
0.6272E−03	0.3000E+01	0.2590E+01	0.0000E+00	−0.3000E+01
0.6355E−03	0.3000E+01	0.2790E+01	0.0000E+00	−0.3000E+01
0.6437E−03	0.3000E+01	0.2990E+01	0.0000E+00	−0.3000E+01
0.6519E−03	0.3000E+01	0.3190E+01	0.0000E+00	−0.3000E+01
0.6600E−03	0.3000E+01	0.3390E+01	0.0000E+00	−0.3000E+01
0.6682E−03	0.3000E+01	0.3590E+01	0.0000E+00	−0.3000E+01
0.6764E−03	0.3000E+01	0.3790E+01	0.0000E+00	−0.3000E+01
0.6845E−03	0.3000E+01	0.3990E+01	0.0000E+00	−0.3000E+01
0.6926E−03	0.3000E+01	0.4190E+01	0.0000E+00	−0.3000E+01
0.7004E−03	0.3000E+01	0.4380E+01	0.0000E+00	−0.3000E+01
0.7085E−03	0.3000E+01	0.4580E+01	0.0000E+00	−0.3000E+01

EXAMPLE

DATA	VGS	VDS		VBS
0.7166E−03	0.3000E+01	0.4780E+01	0.0000E+00	−0.3000E+01
0.7247E−03	0.3000E+01	0.4980E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.4000E+01	0.0000E+00	0.0000E+00	−0.3000E+01
0.1410E−03	0.4000E+01	0.2000E+00	0.0000E+00	−0.3000E+01
0.2720E−03	0.4000E+01	0.4000E+00	0.0000E+00	−0.3000E+01
0.3930E−03	0.4000E+01	0.6000E+00	0.0000E+00	−0.3000E+01
0.5038E−03	0.4000E+01	0.8000E+00	0.0000E+00	−0.3000E+01
0.6044E−03	0.4000E+01	0.1000E+01	0.0000E+00	−0.3000E+01
0.6948E−03	0.4000E+01	0.1200E+01	0.0000E+00	−0.3000E+01
0.7749E−03	0.4000E+01	0.1400E+01	0.0000E+00	−0.3000E+01
0.8447E−03	0.4000E+01	0.1600E+01	0.0000E+00	−0.3000E+01
0.9043E−03	0.4000E+01	0.1800E+01	0.0000E+00	−0.3000E+01
0.9535E−03	0.4000E+01	0.2000E+01	0.0000E+00	−0.3000E+01
0.9925E−03	0.4000E+01	0.2200E+01	0.0000E+00	−0.3000E+01
0.1020E−02	0.4000E+01	0.2390E+01	0.0000E+00	−0.3000E+01
0.1039E−02	0.4000E+01	0.2590E+01	0.0000E+00	−0.3000E+01
0.1047E−02	0.4000E+01	0.2790E+01	0.0000E+00	−0.3000E+01
0.1057E−02	0.4000E+01	0.2990E+01	0.0000E+00	−0.3000E+01
0.1069E−02	0.4000E+01	0.3190E+01	0.0000E+00	−0.3000E+01
0.1080E−02	0.4000E+01	0.3390E+01	0.0000E+00	−0.3000E+01
0.1092E−02	0.4000E+01	0.3590E+01	0.0000E+00	−0.3000E+01
0.1103E−02	0.4000E+01	0.3790E+01	0.0000E+00	−0.3000E+01
0.1115E−02	0.4000E+01	0.3990E+01	0.0000E+00	−0.3000E+01
0.1126E−02	0.4000E+01	0.4190E+01	0.0000E+00	−0.3000E+01
0.1137E−02	0.4000E+01	0.4380E+01	0.0000E+00	−0.3000E+01
0.1149E−02	0.4000E+01	0.4580E+01	0.0000E+00	−0.3000E+01
0.1160E−02	0.4000E+01	0.4780E+01	0.0000E+00	−0.3000E+01
0.1172E−02	0.4000E+01	0.4980E+01	0.0000E+00	−0.3000E+01
0.0000E+00	0.5000E+01	0.0000E+00	0.0000E+00	−0.3000E+01
0.1727E−03	0.5000E+01	0.2000E+00	0.0000E+00	−0.3000E+01
0.3354E−03	0.5000E+01	0.4000E+00	0.0000E+00	−0.3000E+01
0.4878E−03	0.5000E+01	0.6000E+00	0.0000E+00	−0.3000E+01
0.6300E−03	0.5000E+01	0.8000E+00	0.0000E+00	−0.3000E+01
0.7618E−03	0.5000E+01	0.1000E+01	0.0000E+00	−0.3000E+01
0.8832E−03	0.5000E+01	0.1200E+01	0.0000E+00	−0.3000E+01
0.9943E−03	0.5000E+01	0.1400E+01	0.0000E+00	−0.3000E+01
0.1095E−02	0.5000E+01	0.1600E+01	0.0000E+00	−0.3000E+01
0.1185E−02	0.5000E+01	0.1800E+01	0.0000E+00	−0.3000E+01
0.1265E−02	0.5000E+01	0.2000E+01	0.0000E+00	−0.3000E+01
0.1335E−02	0.5000E+01	0.2200E+01	0.0000E+00	−0.3000E+01
0.1391E−02	0.5000E+01	0.2390E+01	0.0000E+00	−0.3000E+01
0.1440E−02	0.5000E+01	0.2590E+01	0.0000E+00	−0.3000E+01
0.1479E−02	0.5000E+01	0.2790E+01	0.0000E+00	−0.3000E+01
0.1507E−02	0.5000E+01	0.2990E+01	0.0000E+00	−0.3000E+01
0.1525E−02	0.5000E+01	0.3190E+01	0.0000E+00	−0.3000E+01
0.1532E−02	0.5000E+01	0.3390E+01	0.0000E+00	−0.3000E+01
0.1545E−02	0.5000E+01	0.3590E+01	0.0000E+00	−0.3000E+01
0.1560E−02	0.5000E+01	0.3790E+01	0.0000E+00	−0.3000E+01
0.1574E−02	0.5000E+01	0.3990E+01	0.0000E+00	−0.3000E+01
0.1588E−02	0.5000E+01	0.4190E+01	0.0000E+00	−0.3000E+01
0.1602E−02	0.5000E+01	0.4380E+01	0.0000E+00	−0.3000E+01
0.1616E−02	0.5000E+01	0.4580E+01	0.0000E+00	−0.3000E+01
0.1630E−02	0.5000E+01	0.4780E+01	0.0000E+00	−0.3000E+01
0.1644E−02	0.5000E+01	0.4980E+01	0.0000E+00	−0.3000E+01

E. Prompt and Response Example

Input your name for identification
===> EXAMPLE

Input data file name
===> EXAMIN : : 29

Input parameter file name
===> FITPAR

Input control file name
===> FITCON

What FNAMR should I store the data in?
===> EXOUT : : 29

Enter any comments (30 characters maximum) now.

F. Example Ouput

FITER — START OF JOB — EXAMPLE

INITIAL VALUES CALCULATED BY PROGRAM

INOGO= 0 FIT ERROR= 0.13483109E−03

NUMBER OF ITERATIONS TAKEN 7

CALCULATED CURRENT IS STORED IN FILE EXOUT : 0: 29

BETA	=	0.17966881E−03
VTO	=	0.54123100E+00
PHI	=	0.36000000E+00
BE	=	0.11326915E+00
ALPHA	=	0.89245571E+00
THETA	=	0.29186574E+00
LAMDA	=	0.90998943E−01
GAMMA	=	0.91554941E−01
DE	=	0.44749537E−01

FITER — NORMAL FINISH — EXAMPLE

APPENDIX J

NPLOT USERS' MANUAL

I. INTRODUCTION

NPLOT is a general-purpose plotter that has been optimized to plot transitor I-V or C-V data formatted in a binary data file. This program plots the output files of FITER, DTTMP, and CFILN directly and, after translation, will plot the binary file from DTACK and DTACQ.

NPLOT is written in Fortran (Hewlett-Packard FTN4X implementation), using HP 1000 graphics plotting software. It was written for use on an HP 1000 minicomputer running the RTE–IVB operating system. The program requires an 83-page partition (22-page code and 61-page EMA) to plot a file up to 25,000 data points in size, 3000 data points plotted during any one pass of the program.

NPLOT is an interactive program that does not require a menu file. NPLOT will not directly produce a hard copy plot; however, hard copy may be obtained using the raster dump capabilities of a graphics terminal.

II. SYSTEM CONSIDERATIONS

The size of this version of NPLOT is 83 pages; however, this size may be decreased if the EMA requirements are decreased. Restricting the maximum file size to a smaller value will decrease the amount of EMA necessary.

NPLOT requires an HP 2648 graphics terminal for operation. The terminal is used as the plotting surface. Optional raster dump ROM is useful because this raster dump is at present the only method of obtaining a hard copy of the plot.

NPLOT is a segmented program. The segments are NPLOT, PDUM, PSET, and PINIT. NPLOT is the main that calls, in turn, PDUM to initialize the plotting device, PINIT, to communicate with the user, and PSET to scale and plot the requested data.

An HP 1000 transfer file is included that will load the program and segments and SP them to a specified disk LU.

To load:

:TR,LDPLOT

The transfer file assumes that the HP 1000 graphics library routines are in the system. If they are not, a system-dependent loader file will have to be created.

III. PLOTTING OPTIONS

By responding to program prompts, the user may verify combinations of the following:

Plot inversion—x and y data are negated

Data filter—Data to plot obtained from within a user-determined window

Nonlinear plot—Either x or y data may be plotted as a function so that $f(x) = a+b*|x|**c$, user to specify a, b and c

Semilog plot—Either log x versus y or log y versus x

Log-log plot–Log x versus log y

Manual scaling—Autoscaling is default.

IV. AXIS SCALING

The autoscaler will attempt to produce an understandable plot of the requested data, but the user may override this by setting values for the plot. The values that must be specified by the user (no defaults) in manual scale mode are:

x min and x max—Minimum and maximum x-axis values

y min and y max—Minimum and maximum y-axis values

x origin and y origin—Location of intersection of the labeled axis

x factor and y factor—Multiply the data by this number to obtain the axis scale values (if the data is 1E−6 and user specifies the min as 0 and max as 2, then the factor is 1E+6

x tic and y tic (minor)—Space between each tic mark

x tic and y tic (major)—Space between labeled tic marks

x label and y label—Units of the plot (i.e., microamps).

In the autoscale mode, the axis may be labeled from femto (1E−15) to tera (1E+12), with tic marks every 0.1, 0.2, 0.25, and 0.5 per division. The autoscaler will fill at least 80 percent of the plotting surface with the plotted data. If the autoscaler becomes confused or if it cannot fill the necessary percentage of the plot surface, it will abort and call in the manual scaler, and the user will have to define the scale values.

The autoscaler works with all of the plot options including autoscaling of log-log and semilog plots.

V. PLOT NOTATIONS

The terminology used throughout this manual and by the program is shown in Figure J-1.

VI. PROGRAM PROMPTING

The following paragraphs describe the program prompting to assist the user in formulating correct reponses. Manual comments are preceded by '--'.

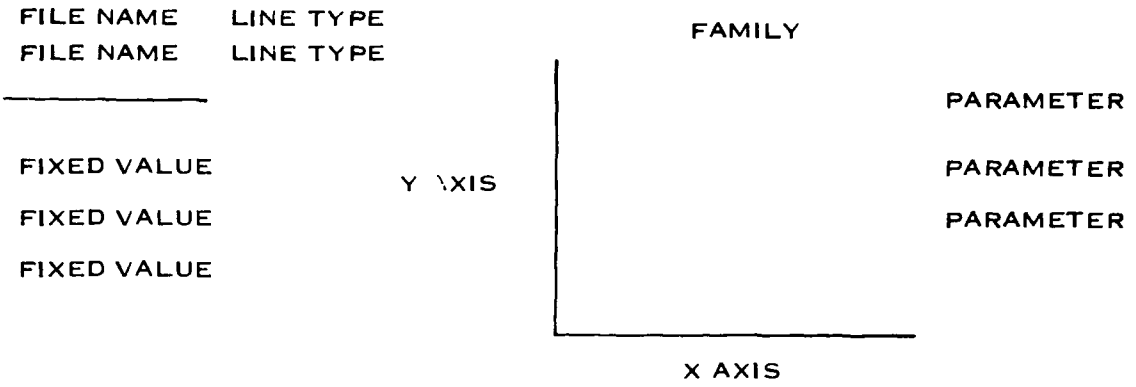
Welcome, what file would you like me to plot?
→ EXAMPL::23 -- full fnamr is valid

File was created by MIKE.MODEL
File was created on day 111 at 14.9 hrs

This file contains these parameters:

NAME	COMMENTS		LOCATION
VDD	FITER	==	X-AXIS
VGG	FITER	==	PARAMETER
VBB	FITER	==	FAMILY
ID	FITER	==	Y-AXIS

The column marked LOCATION is where I will put the parameter on the plot. Possible locations are: X-AXIS, Y-AXIS, FAMILY, PARAMETER, and USER FIXED VALUE.



EXAMPLE: ASSUME A DEVICE TESTED UNDER FOLLOWING CONDITIONS

VDS = 0.0 TO 5.0 BY 0.2 STEP
VGS = 0.0 TO 5.0 BY 1.0 STEP
VBS = 0.0 TO -3 BY -1 STEP
TEMP = -50 TO 125 BY 24 STEP

FOR A STANDARD ID VERSUS VDS CURVE AT 25 DEGREES

ID = CURRENT
VDS = X AXIS
VGS = PARAMETER
VBS = FAMILY
TEMP = FIXED VALUE (25)

Figure J-1. Terms of NPLOT

Do you want to change these locations?
→ N

-- if Y, then program will prompt user with 'NAME →'
-- user to fill in location after the '→' prompt
-- single letter entry is OK

I need specific values for the following:

NAME	COMMENTS		VALUE
VBB	FITER	==	−0.3000E+01

The column labeled VALUE contains the value that I will assign to the specified parameter. If you wish to change the value, type in your value in place of mine.

Do you want to change these values?
→ N

-- if Y, then all possible values are displayed and
-- user is prompted with '→'
-- more than one value may need to be fixed
-- (in notation example fix VBS and TEMP)

If you wish to modify the defaults, enter YES
→ Y -- if N, then following 6 questions are not asked

Would you like to invert the plot?
→ N -- see plotting options

Would you like to limit the data range?
→ N -- see plotting options

Do you want a nonlinear y axis?
→ N -- see plotting options

Do you want a nonlinear x axis?
→ N -- see plotting options

Do you wish to plot the log of Y?
→ N -- see plotting options

Do you wish to plot the log of X?
→ N -- see plotting options
-- last of the defaults

What linestyle do you want?
→ 1 -- possible 0 to 6

XMIN = 0.5000E−01
XMAX = 0.3050E+01
YMIN = 0.0000E+00
YMAX = 0.1496E−02

Do you wish to manually scale the plot?
→ N -- see axis scaling

Do you want to overlay another file?
→ N

-- if Y, then the user will be requested for a new
-- file name to plot.
-- axis scaling will not be changed for overlay

Do you want to plot another file?
→ N -- if Y, then restart program from beginning

Normal completion -- NPLOT

VII. BINARY FILE FORMAT

The following paragraphs describe the file format used by the NPLOT program, intended as a reference for programmers who wish to use the plotting features of NPLOT for data other than transitor parameters. Also included (Addendums A and B) are two sample routines that demonstrate how to use the file format.

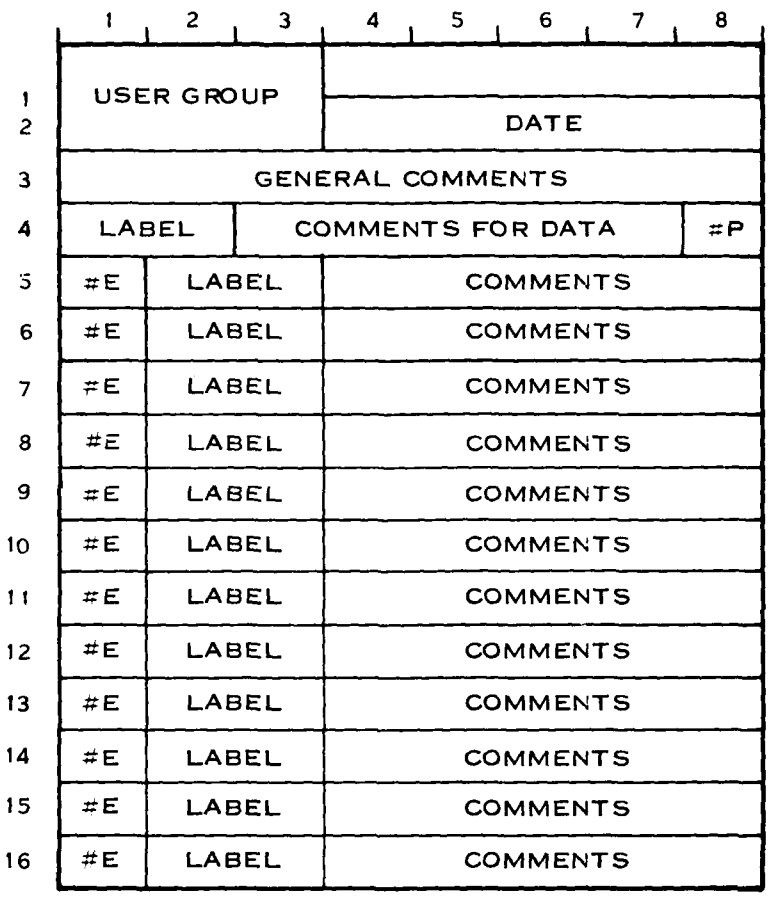


Figure J-2. Words Identifying Parameters

The binary file format used by NPLOT is a type 1 file (128/rec) that has as many blocks as necessary to store the data. Data is arranged serially except for the first few records, which must be formatted as described.

Programs written at this location using this file format allow up to 200 blocks of data to be included in the file. This is a practical restriction, not a theoretical limit.

Record one identifies the creator of the file, contains comments (optional) that describe the contents of the file, and also includes the file date. The space available for the first record determines that up to 12 parameters may be included in the file (Figure J–2).

First 11 integer words identify the user group that created the file (1 to 11)

Next 5 integer words indicate the date (12 to 16)

Next 15 integer words are for user comments (17 to 31)

Next word is the number of parameters (32)

Remaining words are arranged as a logical array (12,8)

First word of each array is the number of elements in the parameter

Next two words are the label used by NPLOT

Remaining 5 words are for user comments or for future use

Each of the above 8 words identify one parameter.

If a parameter is not used, its number of elements (#E) should be set to 0. Note that 12 parameters is the maximum.

Records numbered 2 through total necessary are used to serially store the elements of the parameters. Parameter elements for the first parameter are stored serially until completed, then elements for parameter 2, then elements for parameter 3, . . . parameter 12. The last record used to store the elements of the parameters contains 1E32 as a place holder.

Data items are stored serially in records using function to derive location (Addendum A, column major format of DATA(10,5,4)). Function is such that it accurately describes the storage location used in a multidimensioned array in Fortran.

Function—to find location ARRAY(POS1, POS2, POS3) of maximum ARRAY(MAX 1, MAX 2, MAX 3)

LOCATION = (POS1 − 1) + ((POS2 − 1)*MAX 1) + ((POS3 − 1)*MAX 2) + 1

Addendum A

Function LOCAT returns the absolute location of a multidimensional array element.

```
      INTEGER*4  FUNCTION  LOCAT(NUMMEM,  POSMEM,
      MAXMEM)
      INTEGER*4 COUNT
C
      INTEGER NUMMEM                                    !number of members
      INTEGER POSMEM(NUMMEM),MAXMEM(NUMMEM)   !position and max members
C
C
C
      COUNT = 1
      LOCAT = 1
      DO 100 J = 1,NUMMEM
      LOCAT = ((POSMEM(J)−1) * COUNT) + LOCATE
100   COUNT = COUNT * MAXMEM(J)
      RETURN
      END
$
```

Addendum B

Listing of LDPLOT, transfer file to load and SP NPLOT.

```
:SV,4,,IH
:AN,
:AN,
:AN,
:AN,
:AN,
:AN,          It is assumed that the source file &NPLOT is in the system.
:AN,     What is the cartridge LU that it resides on? (enter ':,LU')
:PA,1
:SE,,1G
:AN,
:AN,     What LU would you like the relocatable code sent to? (enter ':)
:PA,1
:SE,,,1G
:AN,
:AN,     What LU would you like the program to be SP'd on: (enter ':,LU')
:PA,1
:SE,,,,1G
:OF,NPLOT
:OF,PDUM
:OF,PSET
:OF,PINIT
:RU,FTN4X,&NPLOT::2G,0,%NPLOT::3G
:RU,LOADR,,%NPLOT::3G,,LB
:PU,PDUM::4G
:SP,PDUM::4G
:OF,PDUM
:PU,NPLOT::4G
:SP,NPLOT::4G
:OF,NPLOT
:PU,PSET::4G
:SP,PSET::4G
:OF,PSET
:PU,PINIT::4G
:SP,PINIT::4G
:OF,PINIT
:AN,
:AN,                FINISHED SETTING UP NPLOT ON 4G
:SV,0,,IH
```

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